Using PoE PD DC-DC Controllers in the Non-Isolated Buck Configuration

Introduction

Most PoE PD applications use an isolated converter topology, and the available controllers are designed for this configuration. However, they may also be used for non-isolated topologies. The 802.3af/at/bt PoE standards specify input to output isolation, but many low-cost applications comply using other techniques. If the PD system ground is constrained to a single point (the source Ethernet cable), and there are no other connectors and no access to non-isolated conductors, a non-isolated power supply complies with the standard.

There are two configurations possible for the non-isolated Buck. The Buck topology may be configured with Vin(-) as the common input to output connection, or it may be configured with Vin(+) as the common input to output connection. The former is referred to as a low-side Buck, and the latter a high-side Buck; in reference to the location of the common rail. Each has its advantages and disadvantages. Both have the PD/DC-DC controller IC referenced to Vin(-), so either the FET driver output and current sense signal must be level shifted to or from the floating gate-source, or the feedback signal must be level-shifted to IC ground reference Vin(-). For simplification and clarity, V_{IN} is defined as Vin(+) – Vin(-) and V_{OUT} is defined as Vout(+) – Vout(-).

A non-isolated topology reduces the cost and complexity of the power conversion function in a PD, so its appeal is obvious. However, there are some disadvantages to the Buck topology regardless of configuration which will be discussed later in this application note.

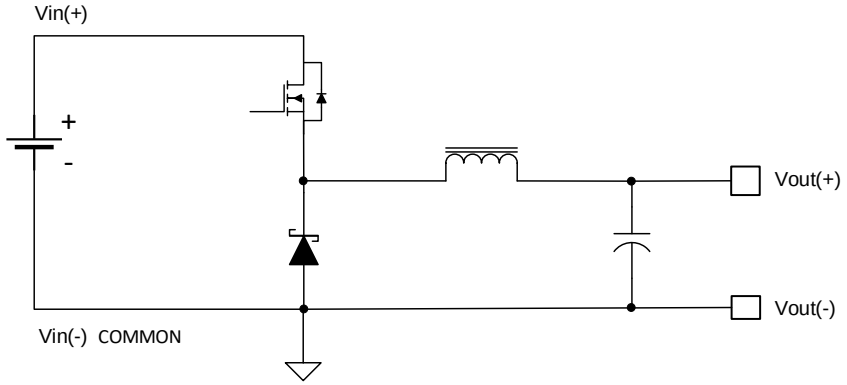

Figure 1. Low-Side Buck Configuration

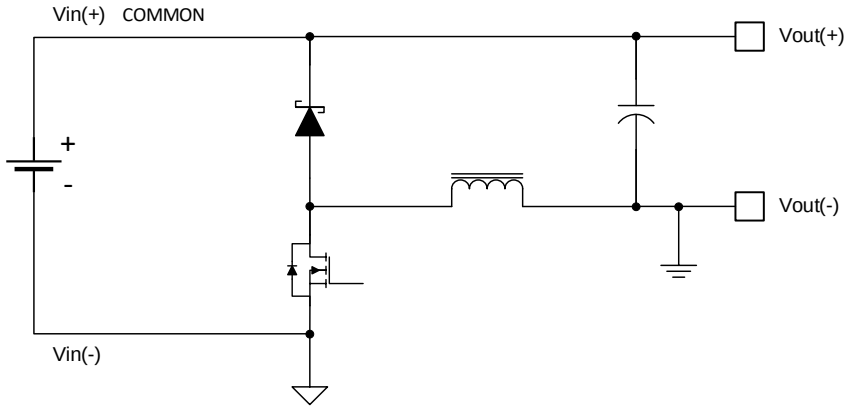

Figure 2. High-Side Buck Configuration

System Design Considerations

The Buck Topology

The 802.3af/at/bt PoE standards require isolation between any accessible conductor, including frame ground if present, and all MDI leads, whether used by the PD or not. Furthermore, any non-MDI connections must be isolated from the MDI leads and all accessible conductors, including frame ground if present. Many low-cost applications, such as VoIP telephones, CCTV cameras, and Wi-Fi access points, use the non-isolated Buck topology. They achieve compliance by having only a single Ethernet cable connection, no other connectors, and no accessible non-isolated conductors.

Aside from safety standards violations which would exist in a non-isolated PD with external cable connections, the PD may not properly operate with a PSE. A PD interconnected with additional equipment may introduce ground loops. Even small ground currents circulating in a multi-point ground system will interfere with PoE Signature Detection due to low signaling currents that are only a few hundred micro-amps.

In an idealized lossless constant frequency non-isolated Buck converter, the duty cycle is equal to Vout/Vin. This ratio can be large in PoE applications. With the maximum input voltage of 57V, a 5V output has a duty cycle of ~9%, and a 3.3V output has a duty cycle of ~6%. Most DC-DC PWM controllers have difficulty producing an ON time of less than 100ns, therefore the narrow duty cycle becomes problematic at higher switching frequencies. The IC controller simply cannot produce a duty cycle with sufficient dynamic range to achieve good output control. However, control laws other than constant frequency, such as constant ON time control, mitigate the problem with the consequence of introducing variable switching frequency operation. Some applications may be sensitive to certain frequency bands and may not tolerate variable frequency operation.

Another difficulty using the Buck topology arises when synchronous rectifier operation is desired. The DC-DC controllers intended for single switch converter topologies require external circuitry to support the second switch operating in complement. IC bridge drivers are available to provide the necessary interface, but the added cost may be unacceptable. Fortunately, PoE applications appropriate to the Buck topology, and having high output current, are not common. Suitable Buck applications are typically Type 1 PDs with output voltages of 5V or greater where the efficiency improvement does not justify the added cost of synchronous rectification.

Low-Side Buck

The low-side Buck converter is by far the most common and recognizable configuration. Virtually every VRM and point-of-load converter falls into this category. The common connection between input and output is the return ground rail to which all voltages are referenced. Applying a single switch PD DC-DC controller requires level shifting two signals. The FET gate drive signal must be shifted from the IC controller to the floating source node of the switching FET, and the FET current signal must be shifted down to the IC controller for over current protection and/or peak current mode control. The level shifting may be accomplished using a discrete network or a transformer or, in the case of the gate drive signal, a half-bridge driver.

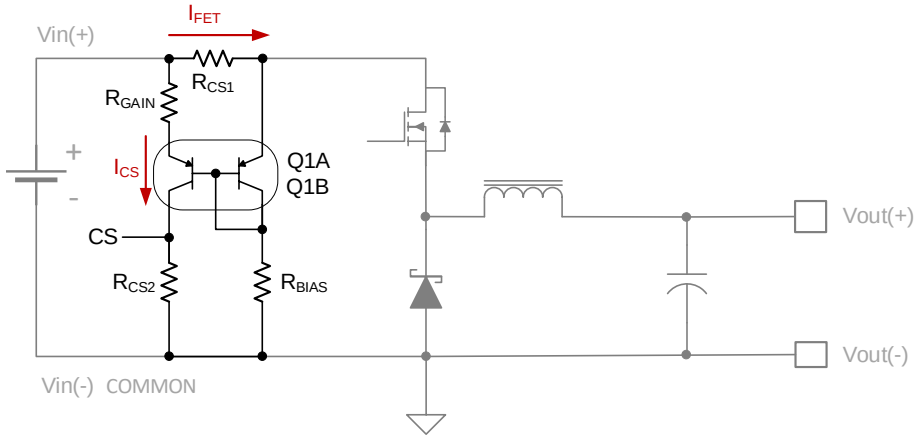

Figure 3. Discrete implementation of FET Current Signal Level Shifting

Figure 3 shows an example of a discrete level shift circuit for the FET current sensing. Transistors Q1A and Q1B are matched PNP devices forming a transistor-diode pair to amplify and translate the current signal to ground. Since there is no need to measure reverse current flow, this circuit has been simplified from a differential pair amplifier by shorting the base-collector junction of Q1B. Sensing resistor R_{CS1} is placed in the drain node to eliminate the common mode switching voltage present at the source node. Voltage CS is the ground referenced current sense signal to be applied to the controller IC.

Q1A and Q1B base-emitter voltages cancel out so that

$$I_{FET} \times R_{CS1} = I_{CS} \times R_{GAIN}$$

and

$$I_{CS} \times R_{CS2} = CS$$

A scaling factor of 1000:1 or higher is used for I_{FET}:I_{CS} to minimize power dissipation in R_{CS1} and Q1. R_{BIAS} sets the base currents for both Q1A and Q1B and is typically large-valued since the base currents are a few micro-amps.

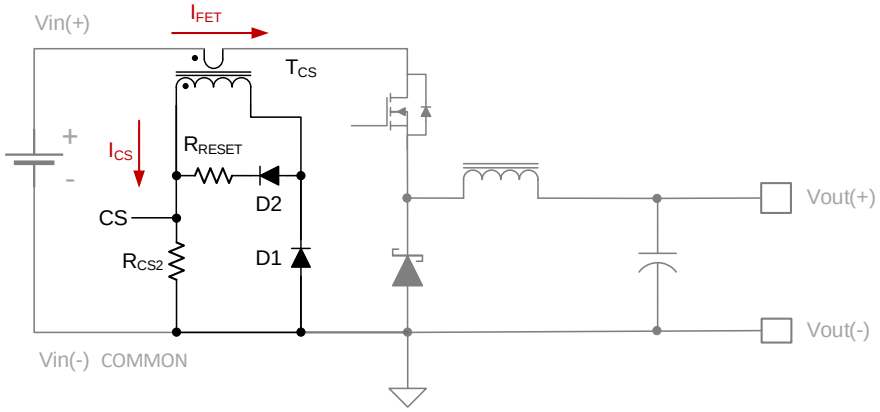

Figure 4. Current Transformer Implementation of FET Current Signal Level Shifting

Alternatively, a current transformer may be used to translate the FET current signal as shown in Figure 4. Transformer T_{CS} has a turns ratio N_P:N_S typically between 1:20 to 1:200. Resistor R_{CS2} creates the CS signal from the rectified secondary current. R_{RESET} and diode D2 allow the transformer to reset during the FET OFF time. Diode D1 should be placed so its V_F does not contribute to the current sense signal amplitude. Although not strictly necessary, T_{CS} is placed in series with the FET drain rather than the source to minimize switching node common mode noise on the signal.

$$I_{FET} \times \frac{N_P}{N_S} \times R_{CS2} = CS$$

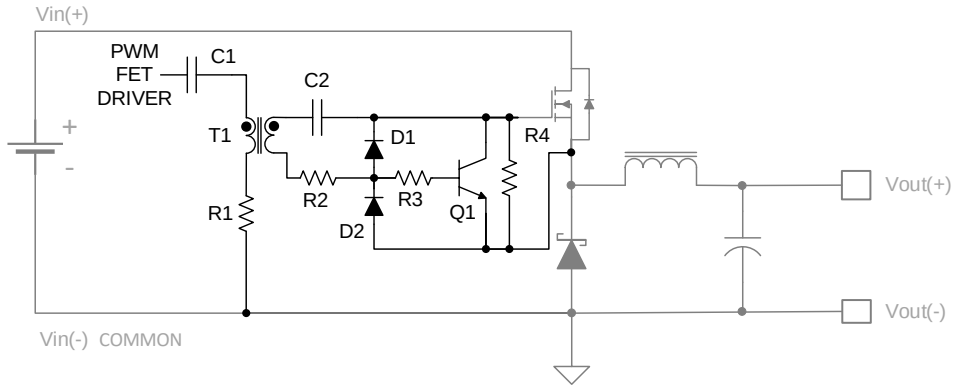

Figure 5. Transformer Coupled Gate Drive for Floating Source FET

A discrete level shifter for driving the floating FET is shown in Figure 5. The PWM ON signal couples through transformer T1 to the FET gate and returns through diode D1B and resistor R2. Capacitors C1 and C2 are DC blocking capacitors which also provide the turn-off voltage when the PWM signal goes low. At turn-off, C2 voltage causes the winding voltage to reverse polarity. With the voltage on C2, transistor Q1 is biased on, shorting the gate-source of the floating FET. R2 is the FET gate resistor, and in combination with R1 provide damping to the LC circuit formed by T1 and capacitors C1 and C2. R3 limits Q1 base current, and with diode D1A, form an anti-saturation network for Q1 to improve its turn-off switching speed.

$$V_F + V_{CE} = V_{BE} + (I_B \times R_3)$$

Since transistor V_{BE} and diode V_F are essentially equal, they cancel each other out and therefore Q1 saturation voltage, V_{CE}, is equal to the voltage drop across R3. The value of R3 determines the level of saturation of Q1, and therefore its storage time. FET turn-on is degraded if Q1 is slow to turn off. Table 1 lists component values. T1 selection depends on the drive signal amplitude, the switching frequency, and the FET V_{GS} threshold voltage.

Table 1. Discrete Floating FET Drive Components.

Reference	Value	Manufacturer
C1	1.0µF, 16V	
C2	0.47µF, 16V	
D1	MMBD914	NXP
D2	SS12	ON Semi
R1	4.99Ω, 0805	
R2	4.99Ω, 0805	
R3	200Ω, 0402	
R4	10.0kΩ, 0402	
T1	Application dependent	Pulse Electronics
Q1	PZT651T1	ON Semi

A half-bridge driver implementation is dependent on the driver selected. Their application requires no discussion beyond the information provided in their respective datasheets and as such, no further discussion shall be provided.

High-Side Buck

The high-side Buck may not appear to be a Buck topology to those unfamiliar with it. However, a quick inspection reveals the two configurations share the same design relationships. During the FET ON time, the voltage across the inductor is $V_{IN} – V_{OUT}$, and during the OFF time (CCM) the voltage across the inductor is $-V_{OUT}$. These ON and OFF time inductor voltage relationships uniquely characterize the Buck converter.

In contrast to the low-side Buck, the high-side Buck requires only level shifting the output voltage feedback signal from the output ground reference to the input ground reference. Fortunately, the level shifting is simple to implement by creating a voltage dependent current source using the output voltage as the control voltage. Figure 6 shows one such implementation using a common base PNP transistor amplifier.

The first step is to select the nominal value of the feedback current source. The current should be high enough so that the transistor Q1 base current is very small by comparison to minimize voltage regulation error, and not so large as to cause significant power dissipation. A value between 200 µA and 1 mA is reasonable. Once the nominal current amplitude is selected, the value of $R_{V\text{-}I\_SET}$ may be calculated.

$$\frac{V_{OUT} - V_{BE\_Q1}}{I_{FB}} = R_{V-I\_SET}$$

Once $R_{V\text{-}I\_SET}$ is determined, and if the base-emitter voltage of Q1 is ignored, it is apparent that I_{FB} will vary in direct proportion to the output voltage. R_{FB} is selected so that I_{FB} at nominal V_{OUT} causes the feedback voltage, V_{FB}, to equal the PD DC-DC converter control loop reference voltage.

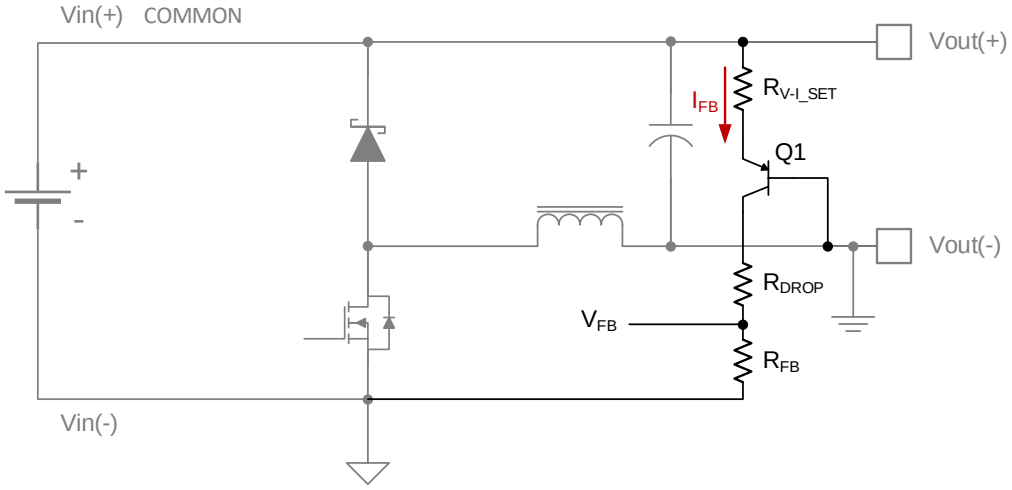

Figure 6. Level Shifting the Feedback Voltage

$$V_{REF} = V_{FB} = R_{FB} \times I_{FB} = R_{FB} \times \left[\frac{V_{OUT} - V_{BE\_Q1}}{R_{V-I\_SET}} - I_{B\_Q1}\right]$$

where:

V_{REF} is the PD DC-DC PWM control loop reference voltage

V_{FB} is the feedback voltage applied to the inverting input of the error amplifier

I_{B_Q1} is the base current of Q1

V_{BE_Q1} is the base-emitter voltage of Q1

R_{DROP} is optional but is used to shift power dissipation away from Q1. Without R_{DROP}, the majority of the voltage drop and power dissipation appear on Q1. R_{DROP} should be sized so that at minimum V_{IN} and maximum V_{OUT} it does not interfere with the feedback current.

$$R_{DROP} \times I_{FB} < VIN(+)_{MIN} - V_{OUT\_MAX} - V_{REF}$$

In practice, the base-emitter voltage and base current of transistor Q1 cannot be ignored. Both are device and temperature dependent and will impact the regulation tolerance. Since the base-emitter voltage varies by ~2.5mV/°C an environmental temperature variation of 50°C, will result in the base-emitter voltage changing by ~125 mV. For a 5V output converter, for example, this translates into a tolerance of 2.5%. A lower output voltage will have higher tolerance. A higher voltage output will have a lower tolerance. Of course, other contributors to regulation must be considered for a complete regulation assessment.

An improved version of the level shifting circuit is shown in Figure 7. Adding a second PNP transistor and configuring it as a diode junction by shorting base-collector, the base-emitter variation cancels out, particularly if a matched pair of PNP transistors is used. The improvement diminishes if the transistors are not matched.

$$\frac{V_{OUT} - V_{BE\_Q1A} + V_{BE\_Q1B}}{I_{FB}} = R_{V-I\_SET}$$

where: V_{BE_Q1A} is the base-emitter voltage of Q1A

V_{BE_Q1B} is the base-emitter voltage of Q1B

R_{FB}, I_{FB}, and R_{DROP} are calculated as in the previous example. R_{BASE} sets the total base current of Q1. The base current must be sufficient for I_{FB} with the worst-case gain and expected output voltage variation. The total base current will be twice this amount since the assumption is the Q1A/B base-emitter voltages and base currents are equal. To ensure proper operation of the circuit, the voltage across R_{BASE} must always be less than Vout(-).

$$R_{BASE} \times I_B < V_{IN} - V_{OUT} - V_{BE}$$

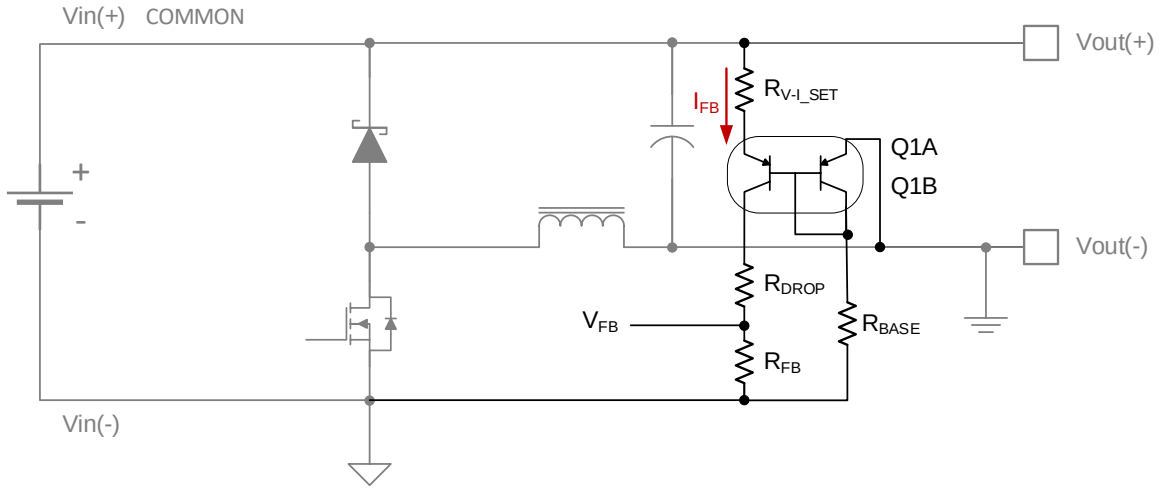

Figure 7. Improved Feedback Level Shifting Circuit

The only disadvantage to the high-side Buck is the voltage offset between input and output grounds. While having a non-common grounding scheme may be psychologically displeasing, the only real difficulty arises when both grounds are accessible, such as during product development debug and possibly some manufacturing assembly steps. Woe betide the individual who mistakenly connects both grounds together with test equipment or ground leads.

Application Schematics

Application schematics for high-side non-isolated Buck converters based on the KTA1137A and KTA1136 PD+DC-DC converter controllers are shown below in Figure 8 and Figure 9, respectively. The designs are virtually identical excepting the differences in the ICs and output power. Due to the similarity of the KTA1137A and KTA1136 non-isolated Buck designs, only performance details for the KTA1136 are provided.

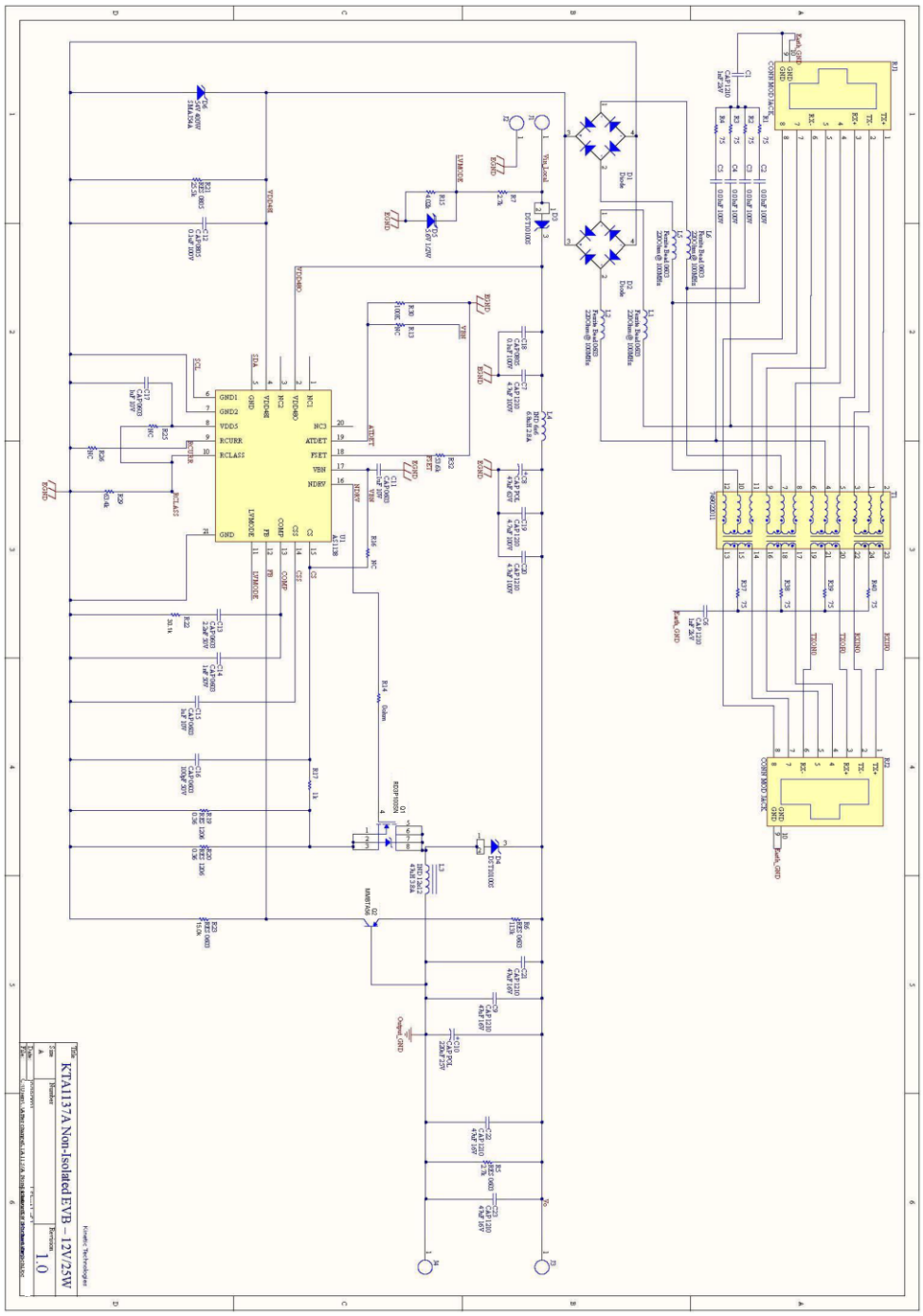

Figure 8. Type 2 PD 12V 2A Non-isolated Buck Converter Based on KTA1137A and Using Method of Figure 6.

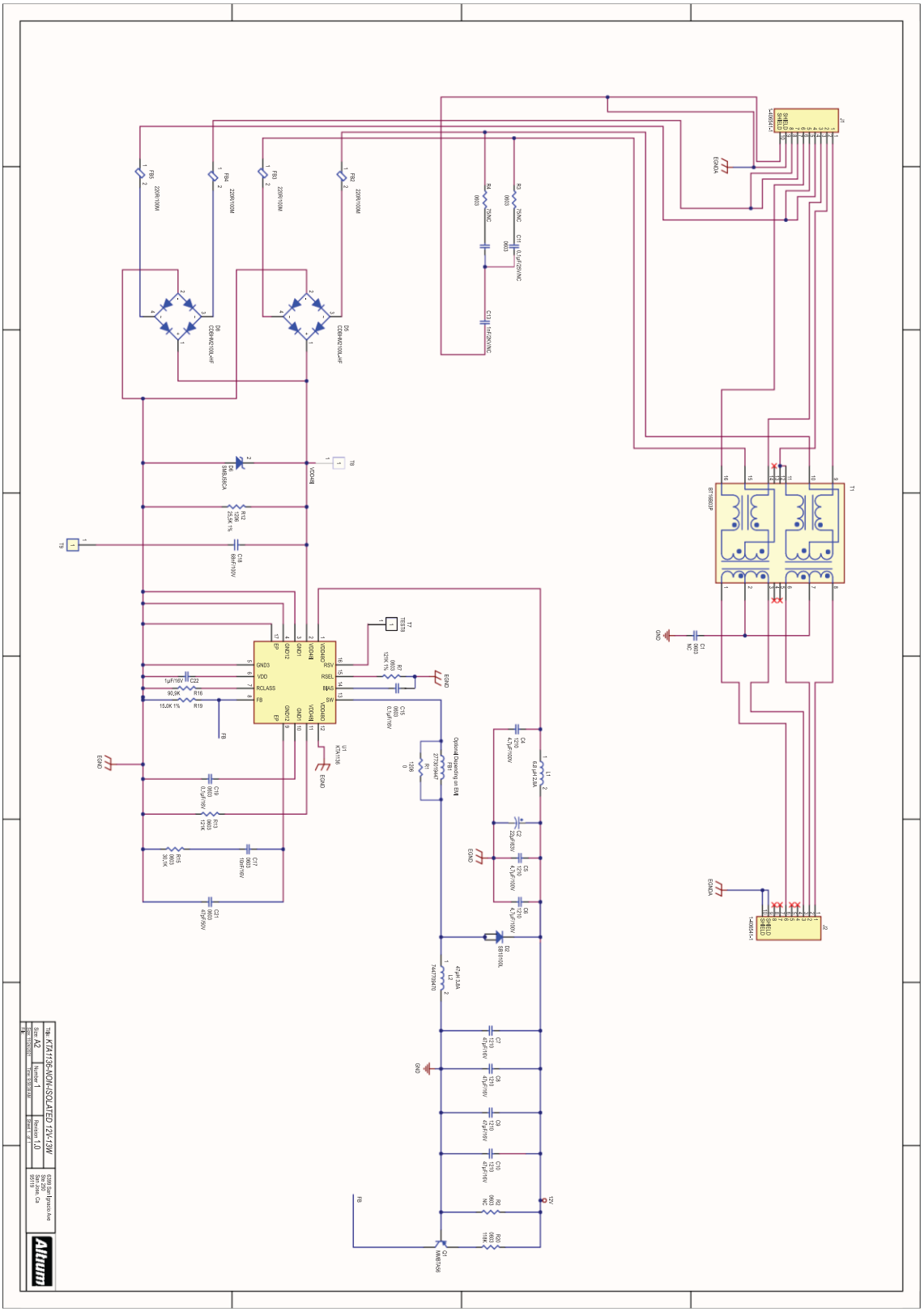

Figure 9. Type 1 PD 12V 1.1A Non-isolated Buck Converter Based on KTA1136 and Using Method of Figure 6.

The KTA1136 non-isolated Buck design provides13W for PoE PD applications. Operating at a switching frequency of 550kHz, it delivers 12V at 1.1A. Performance data follows below.

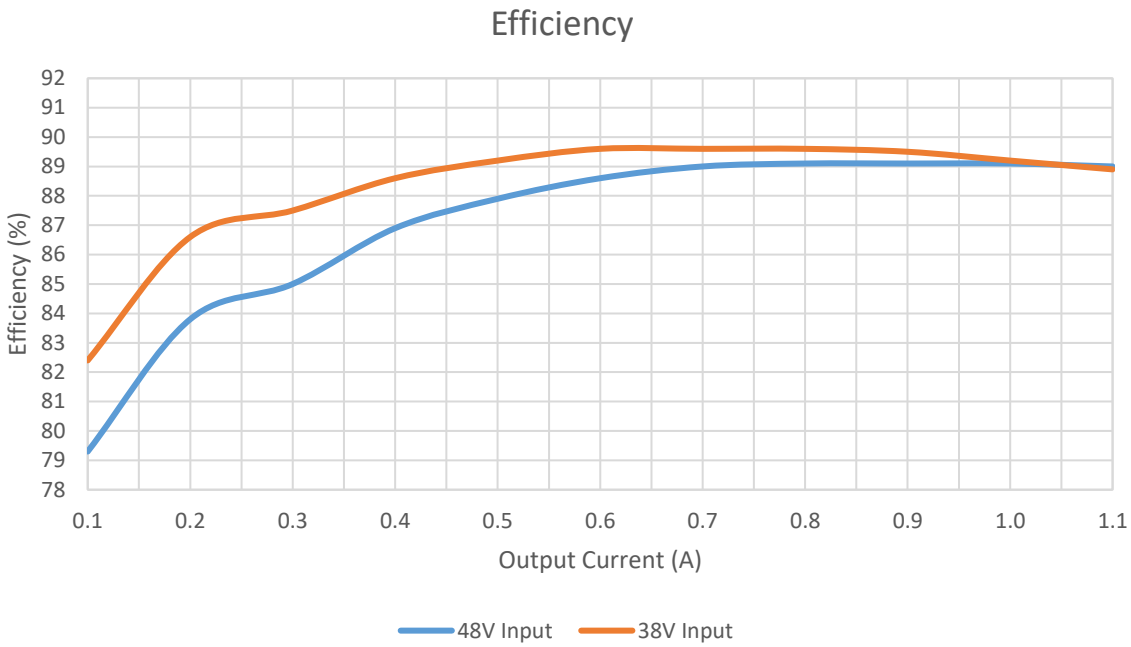

Figure 10. Efficiency Performance for KTA1136 Non-isolated Buck Converter

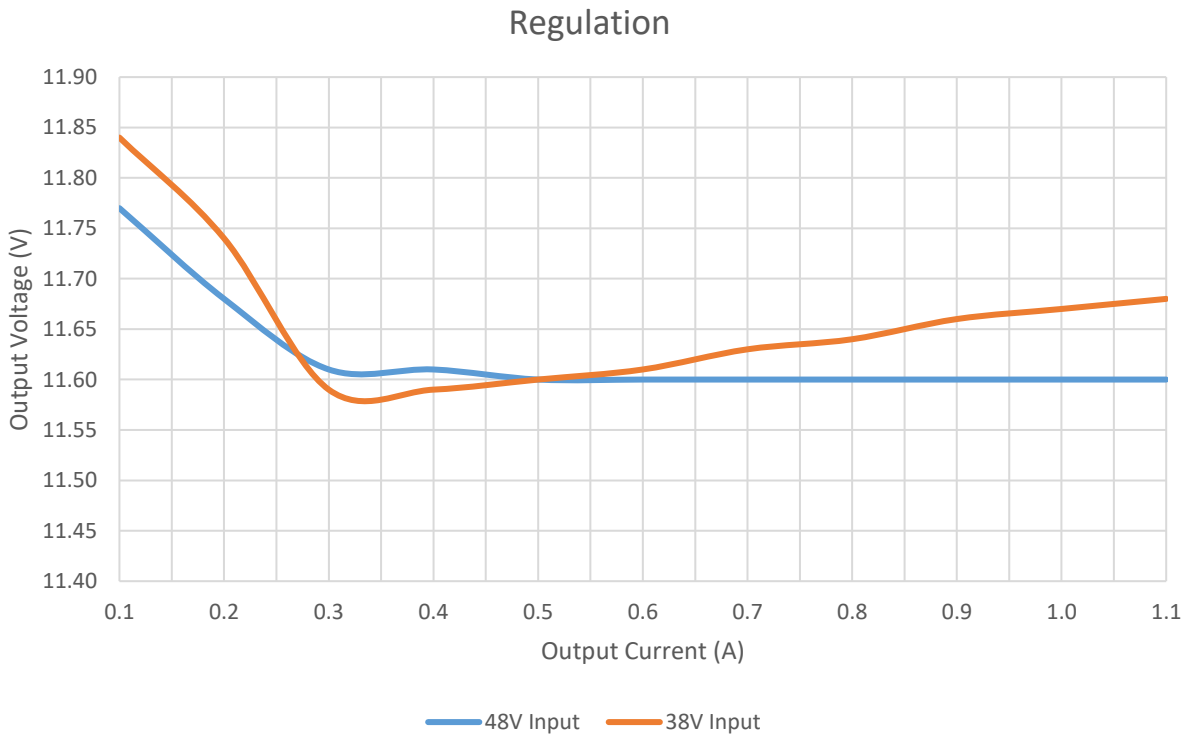

Figure 11. Regulation Performance for KTA1136 Non-isolated Buck Converter

Table 2. KTA1136 BOM

	Quantity	Reference	Description	Value	Package	Manufacturer	Part Number
1	1	C1	CAP CER, 0603 NC	Not Populated	0603		
2	2	C11, C12,	CAP CER, 0603 NC	Not Populated	0603		
3	1	C13	CAP CER, 1210 NC	Not Populated	1210		
4	2	C15, C19	CAP CER, 0.1µF, 16V, X7R, 0603	0.1µF/16V	0603		
5	1	C17	CAP CER, 10nF, 16V, X7R, 0603	10nF/16V	0603		
6	1	C18	CAP CER, 68nF, 100V, X7R, 0805	68nF/100V	0805		
7	1	C2	CAP ELECTROLYTIC, 22µF, 63V, ±20% SM	22µF/100V	8x6.2mm	Panasonic	EEEFK1J220P
8	1	C21	CAP CER, 47pF,50V, COG, 0603	47pF/50V	0603		
9	1	C22	CAP CER, 1µF, 16V, X7R, 0603	1µF/16V	0603		
10	3	C4, C5, C6	CAP CER 4.7µF 100V X7R 1210	4.7µF/100V	1210		
11	4	C7, C8, C9, C10	CAP CER 47µF 16V 1210	47µF/16V	1210		
12	1	D2	Diode Schottky, 10A, 100V	10A/100V	TO277	YIXIN	SB10100L
13	2	D5, D8	Bridge Rectifier Schottky, 2A,100V MBS-2	2A/100V	MBS-2	Comchip	CDBHM2100L-HF
14	1	D6,	Diode TVS, 58V, SMB	58V	SMB	Semtech Corporation	SMBJ58CA
15	1	FB1	BEAD FERRITE, 2SMD, 1LN		2-SMD	Fair-Rite Products Corp.	2773019447
16	4	FB2, FB3, FB4, FB5	BEAD FERRITE, 220 ohm, 0603, 1LN		0603	Murata Electronics	BLM18EG221SN1D
17	2	J1, J2	RJ-45, No LED, tab up, R/A, TH			TE Connectivity	1-406541-1
18	1	L1	IND FIXED, 6.8µH, 2.8A SM	6.8µH/2.8A		Bourns Inc.	SRN6045-6R8Y
19	1	L2	IND FIXED, 47µH, 3A SM	47µH/3.8A		Wurth Electronik	7447709470
20	1	Q1	TRANSISTOR PNP, MMBTA56	80V/500mA	SOT23	ONSemi	MMBTA56LT1G
21	1	R1	RES SMD, 1206 NC	Not Populated	1206		
22	1	R12	RES SMD, 25.5k, 1206, 1%	25.5kΩ	1206		
23	1	R15	RES SMD, 30.1k, 0603, 1%	30.1kΩ	0603		
24	1	R16	RES SMD, 90.9k, 0603, 1%	90.9kΩ	0603		
25	1	R19	RES SMD, 15.0k, 0603, 1%	15.0kΩ	0603		
26	1	R20	RES SMD, 118k, 0603, 1%	118kΩ	0603		
27	3	R2, R3, R4	RES SMD, 0603 NC	Not Populated	0603		
28	2	R7, R13	RES SMD, 0603, 121k, 1%	121kΩ	0603		
29	1	T1	RJ45 LAN Transformer SMD,16PIN RoHS			TNK	BT16B03P

	Quantity	Reference	Description	Value	Package	Manufacturer	Part Number
30	1	U1	KTA1136 PoE 802.3af PD+DC-DC Controller w/Integrated FET		TQFN44-16	Kinetic Technologies	KTA1136

Table 3. KTA1137A BOM

	Quantity	Reference	Description	Value	Package	Manufacturer	Part Number
1	2	C1, C6	CAP CER,2kV,1nF, X7R, 1210	1nF/2kV	1210		
2	4	C2, C3, C4, C5	CAP CER,100V,0.010µF, X7R, 0805	0.01µF/100V	0805		
3	3	C7, C19, C20	CAP CER,100V,4.7µF, X7S, 1210	4.7µF/100V	1210		
4	1	C8	CAP ELECTROLYTIC,63V,47uF, ±20% SM	47µF/63V	8x10.2mm	Panasonic	EEEFK1J470P
5	4	C9, C21, C22, C23	CAP CER,16V,47µF, X5R, 1210	47uF/16V	1210		
6	1	C10	CAP ELECTROLYTIC,25V,220uF, ±20%, SM	220µF/25V	8x10.2mm	Panasonic	EEEFK1E221P
7	3	C11, C15, C17	CAP CER,10V,1µF, X7R, X7R, 0603	1µF/10V	0603		
8	2	C12, C18	CAP CER,100V,0.1µF, X7R, X7R, 0805	0.1µF/100V	0805		
9	1	C13	CAP CER,50V,2.2nF, X7R, 0603	2.2nF/50V	0603		
10	1	C14	CAP CER,50V,1nF, X7R, 0603	1nF/50V	0603		
11	1	C16	CAP CER,50V,100pF, X7R, 0603	100pF/50V	0603		
12	2	D1, D2	Schottky Bridge Rectifiers,100V, 2A, MBS2	2A/100V	MBS2	Comchip	CDBHM2100L-HF
13	2	D3, D4	Diode Schottky,100V,10A, TO277B	10A/100V	TO277B	Littelfuse Inc.	DST10100S
14	1	D5	Diode, Zener,5.6V,500mW, SOD123	5.6V	SOD123	Diodes Inc	BZT52C5V6-7-F
15	1	D6	Diode, TVS, Uni,54 V, 400 W, SMA	54V	SMA	Littlefuse	SMAJ54A
16	2	RJ1, RJ2	CONN MOD JACK 8P8C R/A UNSHLD			TE Connectivity AMP Connectors	5520252-4
17	4	J1, J2, J3, J4	TERM BLK 2P SIDE ENT 2.54MM PCB			TE Connectivity AMP Connectors	282834-2
18	1	L4	Inductor, Fixed, 6.8µH, 2.8A	6.8µH/2.8A		Bourns Inc.	SRN6045-6R8Y
19	4	L1, L2, L5, L6	Bead, Ferrite, 220 ohm, 2A, 0603		0603	Murata	BLM18EG221SN1D
20	1	L3	Inductor, Fixed, 47µH 3.8A SM	47µH/3.8A		Wurth Electronics Inc.	7447709470
21	8	R1-4, R37-R40	Resistor, Chip,75ohm, 5%, 0603	75Ω	0603		
22	2	R5, R7	Resistor, Chip, 5%, 0603, 2.7K	2.7kΩ	0603		
23	1	R6	Resistor, Chip, 113K, 1%, 0603	113kΩ	0603		
24	1	R25	Resistor, Chip, 0603 NC	Not Populated	0603		
25	1	R15	Resistor, Chip, 4.02k, 1%, 0603	4.02kΩ	0603		

	Quantity	Reference	Description	Value	Package	Manufacturer	Part Number
26	3	R13, R14, R16	Resistor, Chip, 0 ohm, 0603	0Ω	0603		
27	1	R17	Resistor, Chip, 1.00k, 1%, 0603	1.00kΩ	0603		
28	2	R19, R20	Resistor, Chip, 0.36 ohm, 1%, 1206	360mΩ	1206		
29	1	R21	Resistor, Chip, 25.5k, 1%, 0805	25.5kΩ	0805		
30	1	R22	Resistor, Chip, 30.1k, 1%, 0603	30.1kΩ	0603		
31	1	R23	Resistor, Chip,15.0k, 1%, 0603	15.0kΩ	0603		
32	1	R26	Resistor, Chip, 0603 NC	Not Populated	0603		
33	1	R32	Resistor, Chip,53.6k, 1%, 0603	53.6 kΩ	0603		
34	1	R29	Resistor, Chip ,63.4k, 1%, 0603	63.4kΩ	0603		
35	1	Q1	FET, 100V 10A, LL Gate, TO-252	100V/10A	TO252	Rohm Semi	RD3P100SNTL1
36	1	Q2	TRANSISTOR PNP, MMBTA56	80V/500mA	SOT23-3	ONSemi	MMBTA56LT1G
37	1	T1	Transformer, LAN 10/100/1000 PoE			Wurth Electronics Inc.	749022011
38	1	U1	KTA1137A IEEE 802.3af/at PoE PD+DC-DC Controller		TQFN55-20	Kinetic Technologies	KTA1137A

Summary

The non-isolated Buck topology may be applied to PoE PDs and remain compliant with 802.3af/at/bt providing all voltages and non-isolated conductors are inaccessible. Applying standard PD DC-DC converter controller ICs requires level shifting some control signals either to or from the IC controller ground reference. Of the two configurations, the high-side Buck is less complex and has lower cost.

Related Documentation

1. Kinetic Technologies KTA1137A Datasheet
2. Kinetic Technologies KTA1136 Datasheet

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