Active Clamp Current-Mode PWM Controller

Features

- Fully supports IEEE® Std. 802.3bt
- PWM peak current mode controller
- Dual low side gate driver
- High efficiency topologies:
  - Flyback, Forward
  - Flyback with synchronous rectification
  - Flyback with active clamp
  - Forward with active clamp
- Wide VIN Range: 8V to 80V
- >1.5A Output Gate Drive Capability
- Programmable fixed frequency up to 1MHz
- Integrated Short-Circuit Protection.
- Programmable Soft Start Time
- Programmable dead time between G1 and G2
- Programmable slope compensation
- Internal pull-up resistor in feedback for optocoupler and isolated connection
- Over current, OV/UVLO, and thermal Protection
- Programmable Frequency Dithering for Low EMI Spread-Spectrum Operation
- Synchronous External Clock
- Soft turn off
- Maximum duty cycle limit
- Internal high voltage start-up regulator
- -40°C to +125°C Junction Temperature Range
- Small 3mmx3mm WQFN Package

Brief Description

The KTB2140 is a PWM controller that integrates all the circuitry required to design a smart and efficient converter for PoE and telecom small and mid-powered applications.

KTB2140 features a programmable oscillator for the switching frequency, adjustable slope compensation, dual low-side drivers with programmable dead time, programmable soft-start, soft-stop, programmable frequency dithering, and maximum duty limit.

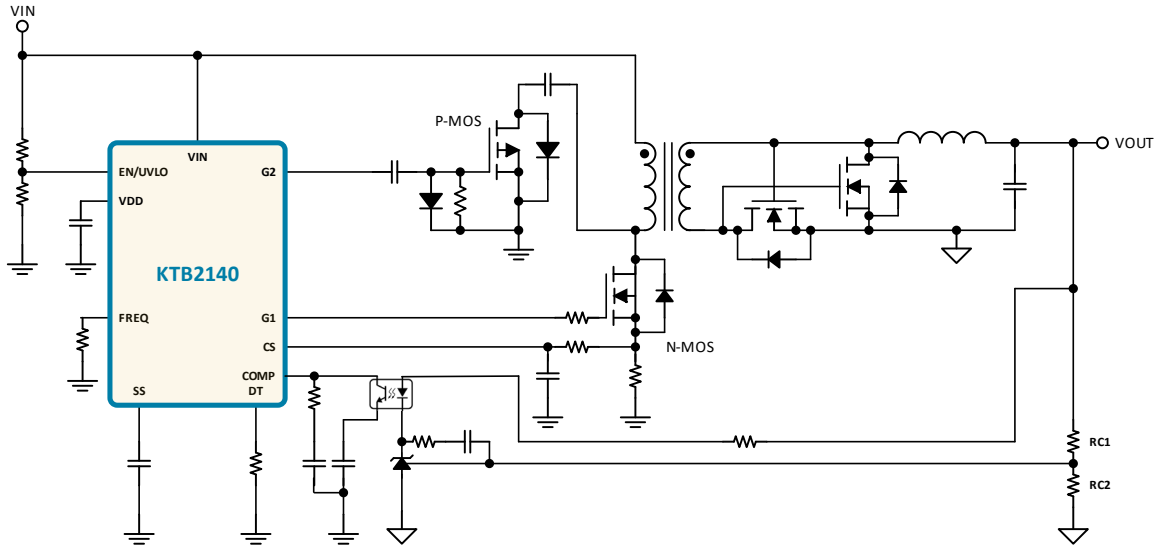
An internal high-voltage linear regulator allows the device to start up with a minimum number of external components. There are dual low side gate drivers that are mainly for active clamp forward application. When the second driver is not used in low power flyback converters, it can be floating.

The KTB2140 device embeds a set of protections that enable the design of a self-protected converter. It also targets high efficiency conversion at a wide range of loads.

Applications

- PoE Powered Devices
- Up to 200 Watt SMPS
- Voice over IP (VoIP) Phones
- Lighting and High-Power Wireless Data Systems
- Wireless LAN Access Points, WiMAX Terminals
- Point-of-sale (POS) Terminals, RFID Terminals
- Thin Client and Notebook Computers
- Fiber-to-the-home (FTTH) Terminals

Typical Application

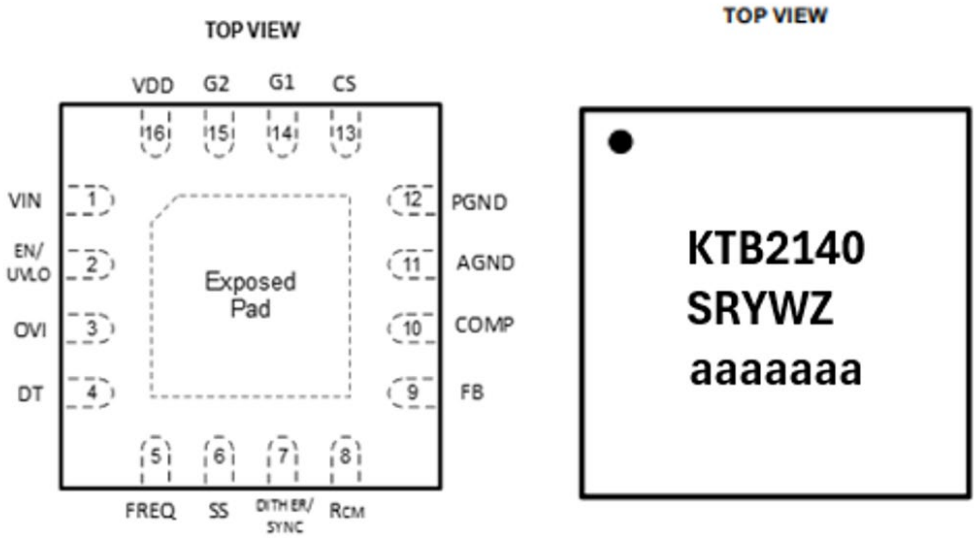


Ordering Information

Part Number	Marking[1]	Auxiliary Drive Mode	Operating Temperature	Package
KTB2140GUAP-TB	SRYWZ	G2 for PMOS	-40°C to +125°C Junction Temperature	WQFN33-16

Pinout Diagram

WQFN33-16



3.00mm x 3.00mm x 0.75mm
Top Mark: SR = Device Code, YW = Date Code, Z = Serial Number
aaaaaaa = Serial Number of Assembly Lot

1 "SR" is the device code, "YW" is the date code, "Z" - Serial Number.

Pin Descriptions

Pin #	Name	Function
1	VIN	High-voltage input.
2	EN/UVLO	Enable, and undervoltage detection and protection.
3	OVI	Input voltage reference for overvoltage detection and protection.
4	DT	Dead time or delay between gate signals.
5	FREQ	Switching frequency set. An external resistor connected from FREQ to AGND can set the oscillator frequency.
6	SS	Soft-start set. A capacitor connected from this pin to AGND sets the converter soft-start time. Use of stable ceramic capacitors is recommended.
7	DITHER /SYNC	Frequency dithering programming or synchronization connection. DITHER: For spread-spectrum frequency operation and improved EMI by using internal oscillator. Connect a capacitor from DITHER to AGND and a resistor from DITHER to FREQ pins. SYNC: Use this pin to synchronize the internal oscillator to the externally applied frequency.
8	RCM	Slope compensation programming input and resistor. A resistor connected from this pin to AGND programs the amount of internal slope compensation. Can not be floating.
9	FB	If we use internal E/A for the part, this FB pin will be the input of E/A.
10	COMP	Comp pin to control the target output voltage. This pin will be output of E/A. Connect the compensation network between COMP and AGND for non-isolated applications. Connect optocoupler output to COMP directly for isolated applications.
11	AGND	Analog ground pin.
12	PGND	Power Ground Pin.
13	CS	This pin is used to sense the peak current utilized for current mode control and for current Limiting/protection functions.
14	G1	Main gate driver output of the PWM controller.
15	G2	Secondary gate driver output. AUX gate driver output for active clamp or synchronous rectification designs.
16	VDD	Output of the internal high-voltage regulator.

Absolute Maximum Ratings[2]

(T_A = 25˚C unless otherwise noted)

Symbol	Description	Value	Units
V_{IN}	VIN to AGND	-0.3 to 100	V
EN	EN to AGND	-0.3 to 100	V
VDD	VDD to AGND	-0.3 to 16	V
G1, G2	Gate1, and Gate 2 to PGND	-0.3 to VDD+0.3	V
DT, FREQ, CS, SS	DT, FREQ, CS, SS to AGND	-0.3 to 6	V
FB, COMP, OVI, RCM, SYNC	FB, COMP, OVI, RCM, SYNC to AGND	-0.3 to 6	V
T_S	Storage Temperature	165	°C
T_J	Junction Operating Temperature	-40 to 150	°C

ESD Ratings

Symbol	Description	Value	Units
V_{ESD_HBM}	JEDEC-JS-001 Human Body Model (HBM)[3]	2	kV
V_{ESD_CDM}	JESD22-C101, Charged device model (CDM), All pins	0.5	kV

Thermal Capabilities[4]

Symbol	Description	Value	Units
θ_{JA}	Thermal Resistance – Junction to Ambient	76.4	°C/W
P_D	Maximum Power Dissipation	1.3	W
$\Delta P_D/\Delta T$	Derating Factor Above T_A = 25°C	-13.1	mW/^{O}C

Recommended Operating Conditions[5]

Symbol	Parameter	Min.	Typ.[6]	Max.	Units
V_{IN8}	Input Power Supply	8	-	80	V
T_A	Ambient Operating Temperature Range	-40	-	+85	°C
T_{J_MAX}	Recommended Maximum Junction Operating Temperature			125	°C

2. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
3. Human Body Model and Charged Device Model ESD limits are specified at the chip level.
4. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.
5. The recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Kinetic does not recommend exceeding them or designing to Absolute Maximum Rating.
6. Typical specification, not 100% tested. Performance guaranteed by design and/or other correlation methods.

Electrical Characteristics[7]

Unless otherwise noted, specifications are for T_J = -40°C to +125°C. Typical specifications are for T_J = +25°C and V_{IN} = 48V, Typical specifications not 100% tested.

Supply Specifications (VIN)

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage		8	48	80	V
I_{VIN_NOSW}	No switching current	VIN = 48 V, VFB = 1.24V		1		mA
I_{VIN-SD}	Shutdown current	VIN = 48 V, VEN = 0 V		6		µA
V_{OVI_R}	Input Over Voltage Protection with 1.5% voltage divider	V_{OVI} Rising	1.19	1.24	1.31	V
V_{OVI_F}		V_{OVI} Falling	1.05	1.13	1.18	V
V_{UV-R}	Input Under Voltage Protection	Vin Rising		5	5.4	V
V_{UV-F}		Vin Falling	4.2	4.8		V

VDD

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{VDD}[8]	VDD regulation	14 V ≤ VIN ≤ 75 V	9	10	11	V
	Regulation Disabled	6 V ≤ VIN < 14 V		V_{IN}-1.3		V
I_{VDD}	Supply current			20		mA
$I_{VDD-LIM}$	VDD current limit	VDD = 0 V		50		mA
V_{VDD-OV}	VDD clamped voltage			15		V

Error Amplifier

Symbol	Description	Conditions	Min	Typ	Max	Units
GBW[9]	Gain Bandwidth			10		MHz
A_{CC}[9]	DC Gain			65		dB
A_{GM}[9]	Error Amplifier Transconductance	V_{FB} = 1.24 V, V_{COMP} = 1 V	80	120	150	µS

Feedback (FB)

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{FB}	FB Pin Voltage		1.215	1.240	1.265	V

Enable (EN)

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{EN}	Turn-on threshold		1.14	1.24	1.29	V
V_{EN-HYS}	Hysteresis			80		mV

7 Device is guaranteed to meet performance specifications over the –40°C to +125°C Junction temperature range by design, characterization, and correlation with statistical process controls.

8 VDD provides bias for the internal gate drive.

9 Guaranteed by design.

Current Limit

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{CSD}	Current limit threshold Default		260	300	340	mV
T_{BLK}	Leading edge blanking time			65		ns
T_{DL}	Delay to Driver			20		ns

Soft-Start/Soft Stop (SS)

Symbol	Description	Conditions	Min	Typ	Max	Units
I_{SSC}	Soft start charger current			10		µA
I_{SSD}	Soft-stop Dis-charger current			10		µA
T_{SSD}	Soft Start delay			1		ms
T_{SS}	Soft start	Css=100nF	1		30	ms
T_{ST}	Soft Stop	Css=100nF	1		30	ms

PWM

Symbol	Description	Conditions	Min	Typ	Max	Units
D_{MIN} [9]	Minimum duty cycle	(Burst mode)		0		%
	Minimum duty cycle	(CCM mode for Fsw= 370KHz)			5	%
D_{MAX} [9]	Maximum duty cycle	For VIN = 48V, DT = 0nS	75	82	89	%

Oscillator (FREQ)

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SW}	Freq Range		100		1200	KHz
	Default Frequency	Rfreq = 62k		370		KHz
	Fsw accuracy	Rfreq = 62k	-10		10	%

Dead Time

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{DT}	Dead Time Range	Based on Resistance value	10		450	ns
	Default dead Time	RDT=130K		280		ns

Synchronization (default is not connected)

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{DELAY}	Sync to output delay	Rfreq=62K， RDT=130K		700		ns
	Syn Freq Range	Sync Freq range is based on Frequency pin setting	1.1xFsw		1.3xFsw	kHz

Gates Driver

Symbol	Description	Conditions	Min	Typ	Max	Units
T_R	Rise Time	CLOAD = 2.0nF, VDD = 10 V		15		ns
T_F	Fall Time	CLOAD = 2.0nF, VDD = 10 V		15		ns
	Peak current Source			1.5		A
	Peak current Sink			1.5		A

Electrical Characteristics (continued)[10]

Unless otherwise noted, specifications are for T_A = -40°C to +125°C. Typical specifications are for T_A = +25°C and V_{IN} = 48V, Typical specifications not 100% tested.

Dithering Ramp Generator

Symbol	Description	Conditions	Min	Typ	Max	Units
	Charging Current			50		µA
	Discharging Current			50		µA
	Ramp High Trip			2		V
	Ramp Low Trip			0.4		V

Ramp/Slope Compensation

Symbol	Description	Conditions	Min	Typ	Max	Units
I_{SLOPE}	Slope Bias Current			10		µA
R_{SLOPE}	Slope resistor range		20		200	KΩ
	Slope Compensation ramp	For RCM=100KΩ (slope = 5mV/µs per KΩ)		500		mV/ µs

Over Temperature Protection (OTP)

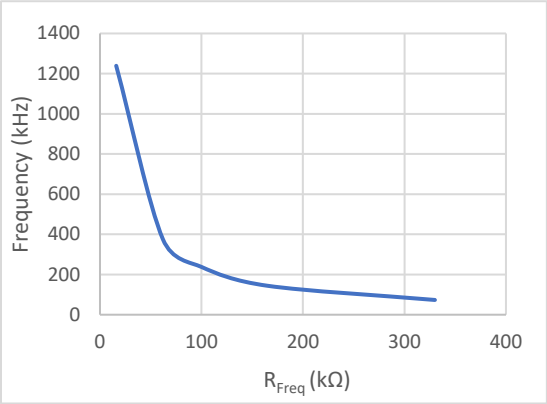
Symbol	Description	Conditions	Min	Typ	Max	Units
T_{sd}	Thermal shutdown threshold		140	150	160	°C
	Hysteresis			20		°C

10. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization, and correlation with statistical process controls.

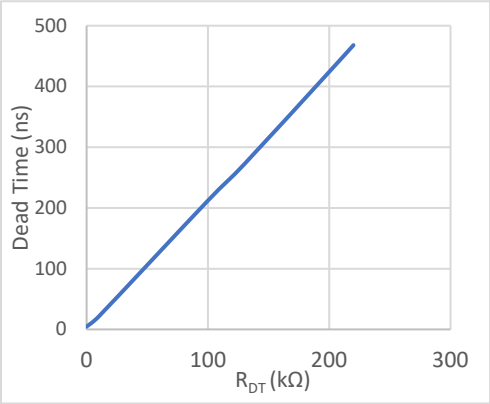
Typical Characteristics

V_{IN} = 48V, R_{FREQ} = 62k, R_{dt} =130K, R_{rcm} =100K, T_A = 25°C, unless otherwise specified.

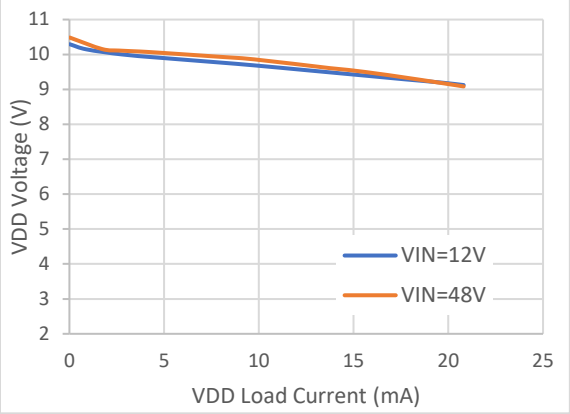
Switching Freq. vs. Programming Resistance



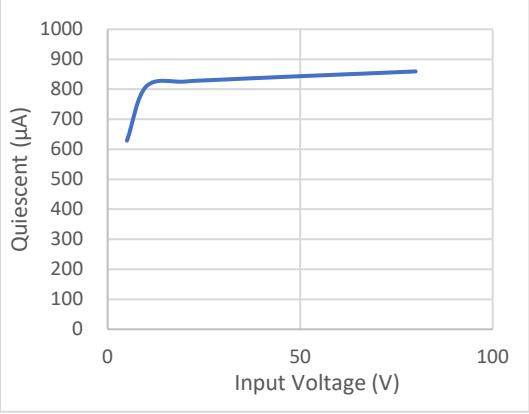
Dead Time vs. Programming Resistance



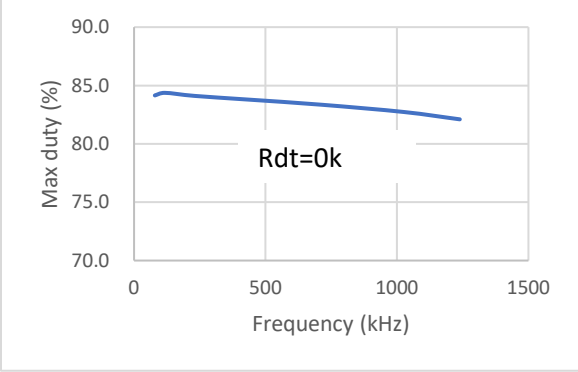
VDD Voltage vs. VDD Load Current



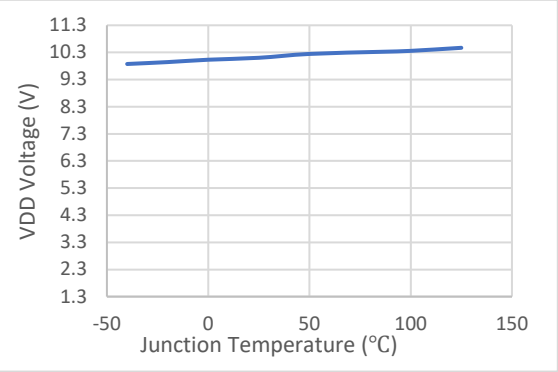
Quiescent Current vs. Input Voltage



Max. Duty with Frequency



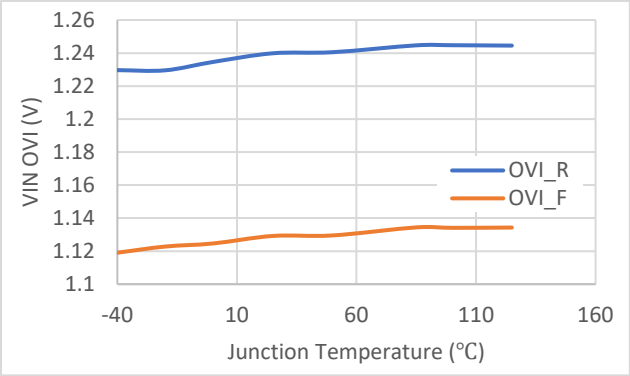
VDD Voltage vs. Junction Temperature



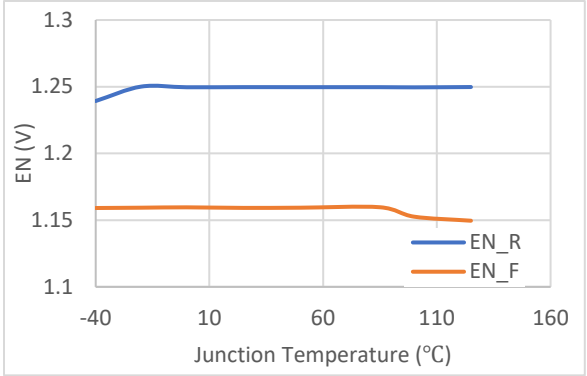
Typical Characteristics (continued)

V_{IN} = 48V, R_{FREQ} = 62k, R_{dt} =130K, R_{rcm} =100K, T_A = 25°C, unless otherwise specified.

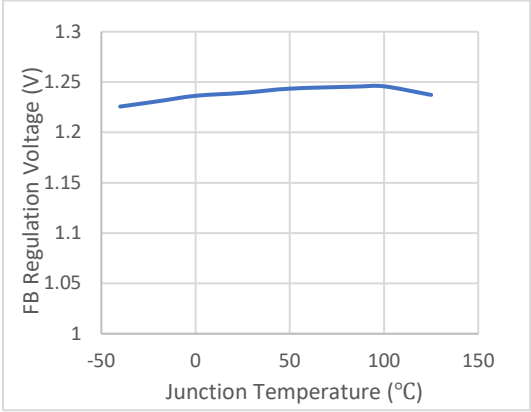
VIN OVI vs. Junction Temperature



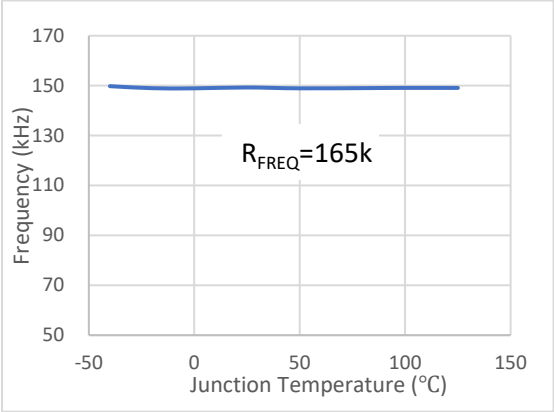
EN/UVLO vs. Junction Temperature



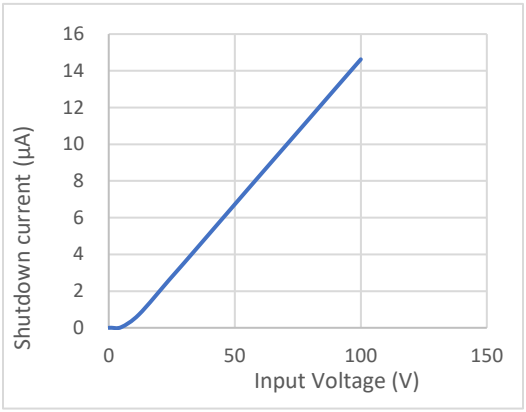
FB Regulation Voltage vs. Temperature



Frequency vs. Junction Temperature



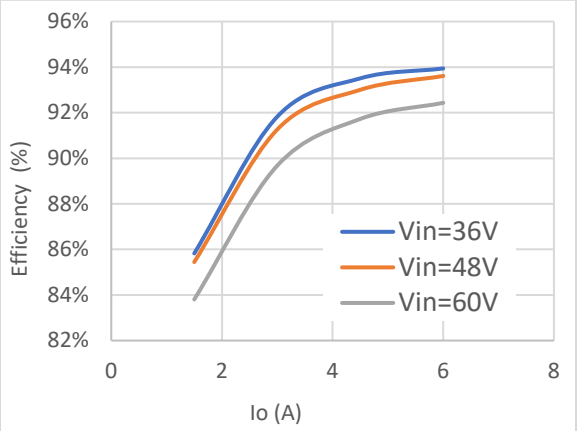
Shutdown Current vs. Input Voltage



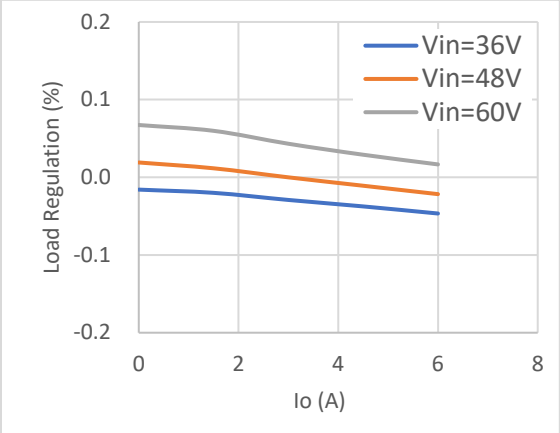
Typical System Performance Characteristics

V_{IN} = 36V-60V, V_{OUT} = 12V, I_{OUT} = 6A; R_{FREQ} = 62K, R_{dt} = 130K, R_{rcm} = 100K, T_a = 25°C unless otherwise specified.

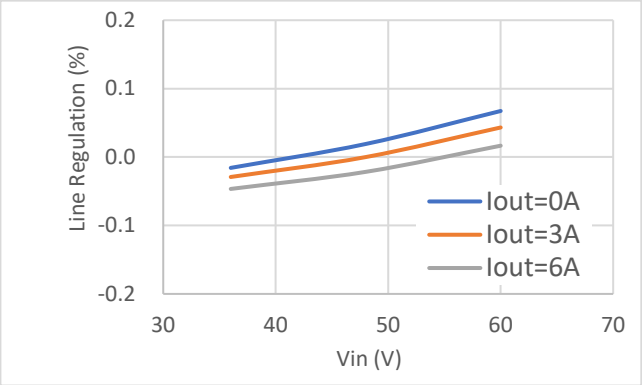
Efficiency



Load Regulation



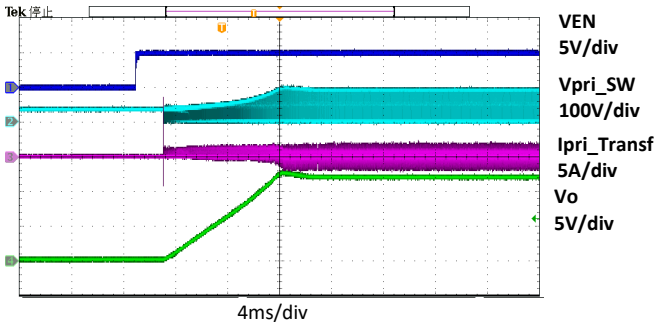
Line Regulation



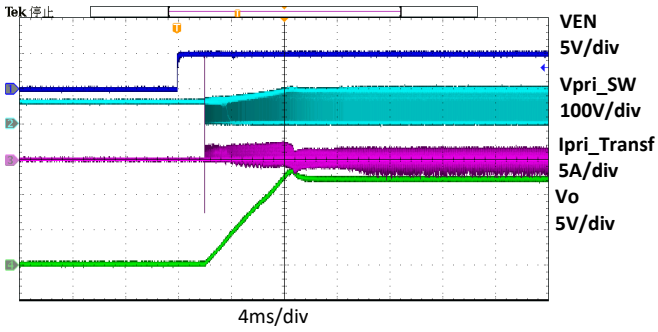
Typical System Performance Characteristics (continued)

V_{IN} = 36V-60V, V_{OUT} = 12V, I_{OUT} =6A; R_{FREQ} = 62K, R_{dt} = 130K, R_{rcm} = 100K, T_a = 25°C unless otherwise specified.

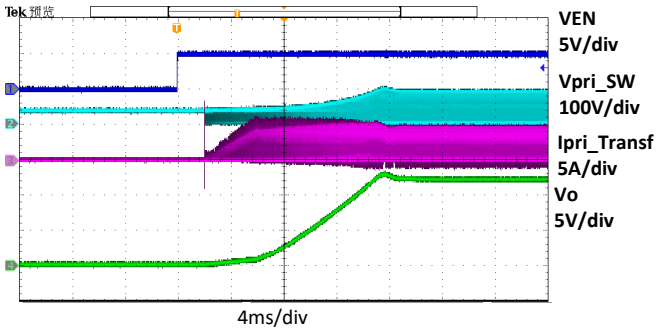
Enable Turn On
(36V_{IN}, 12V_{OUT}, I_{OUT} = 0A)



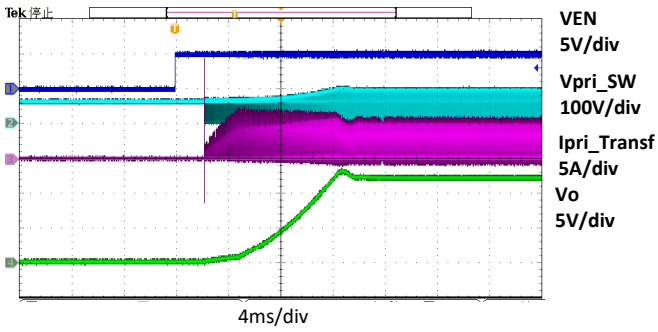
Enable Turn On
(60V_{IN}, 12V_{OUT}, I_{OUT} = 0A)



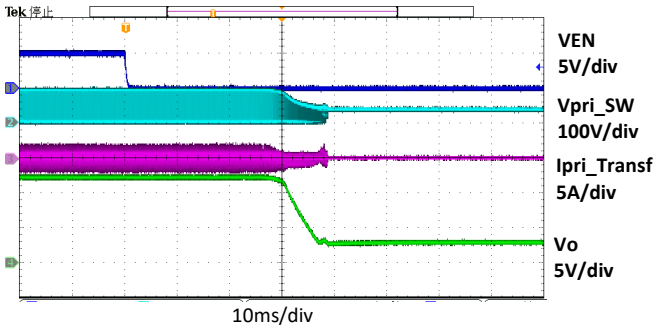
Enable Turn On
(36V_{IN}, 12V_{OUT}, I_{OUT} = 6A)



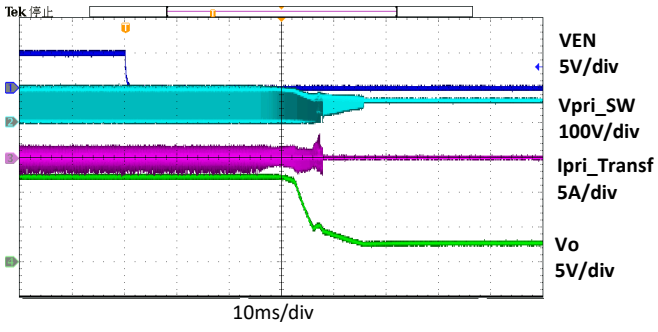
Enable Turn On
(60V_{IN}, 12V_{OUT}, I_{OUT} = 6A)



Enable Turn Off
(36V_{IN}, 12V_{OUT}, I_{OUT} = 0A)



Enable Turn Off
(60V_{IN}, 12V_{OUT}, I_{OUT} = 0A)

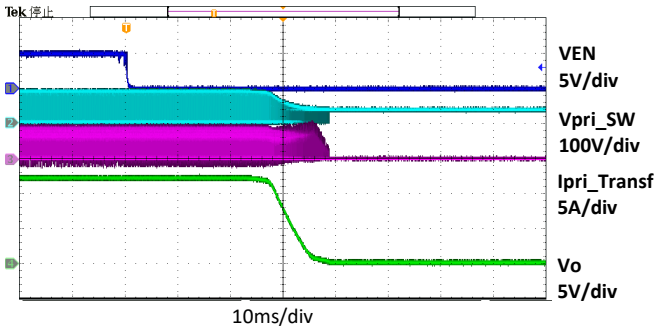


Typical System Performance Characteristics (continued)

V_{IN} = 36V-60V, V_{OUT} = 12V, I_{OUT} =6A; R_{FREQ} = 62K, R_{dt} = 130K, R_{rcm} = 100K, T_a = 25°C unless otherwise specified.

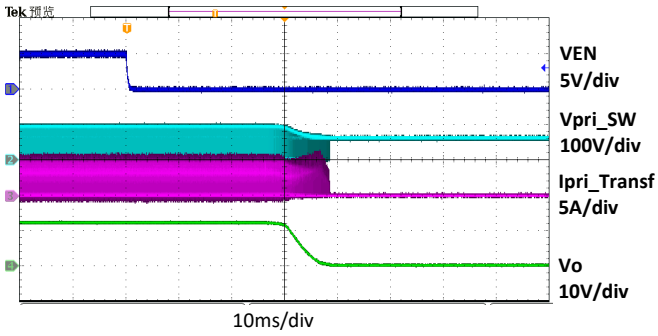
Enable Turn Off

(36V_{IN}, 12V_{OUT}, I_{OUT} = 6A)



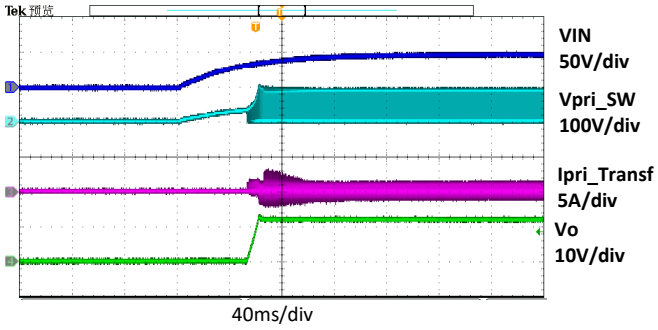
Enable Turn Off

(60V_{IN}, 12V_{OUT}, I_{OUT} = 6A)



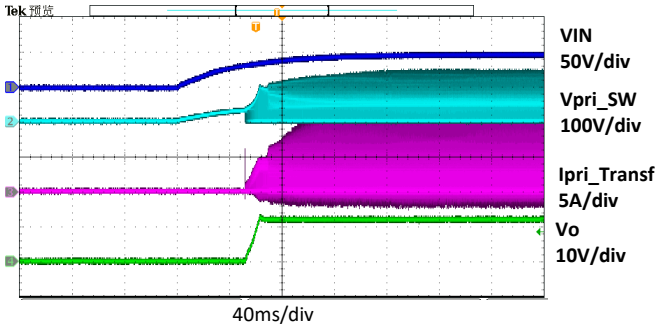
Input Startup

(48V_{IN}, 12Vo, Io = 0A)



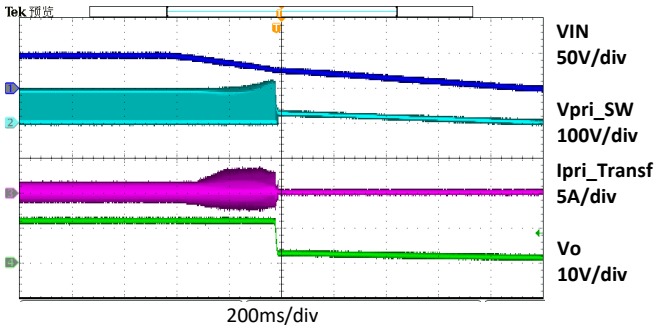
Input Startup

(48V_{IN}, 12V_{OUT}, I_{OUT} = 6A)



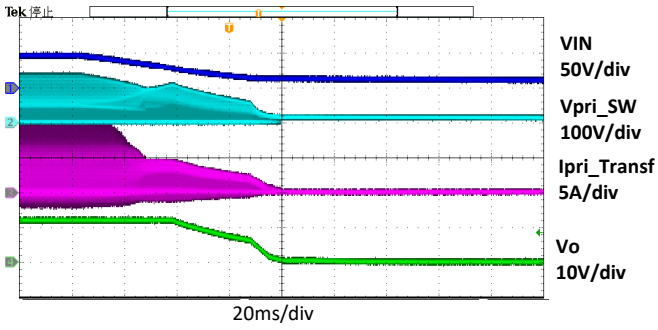
Input Shutdown

(48V_{IN}, 12V_{OUT}, I_{OUT} = 0A)



Input Shutdown

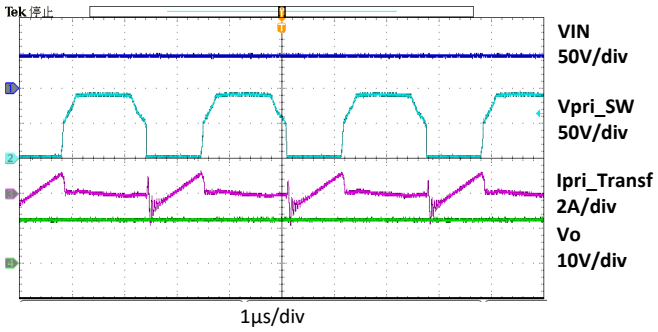
(48V_{IN}, 12V_{OUT}, I_{OUT} = 6A)



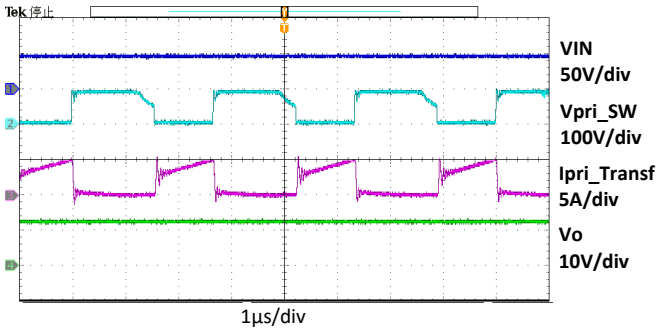
Typical System Performance Characteristics (continued)

V_{IN} = 36V-60V, V_{OUT} = 12V, I_{OUT} =6A; R_{FREQ} = 62K, R_{dt} = 130K, R_{rcm} = 100K, T_a = 25°C unless otherwise specified.

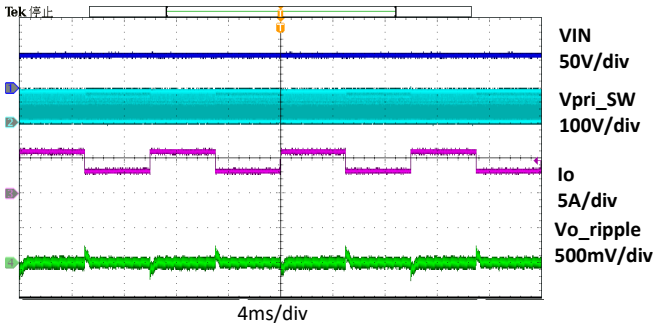
Steady State
(48V_{IN}, 12V_{OUT}, I_{OUT} = 0A)



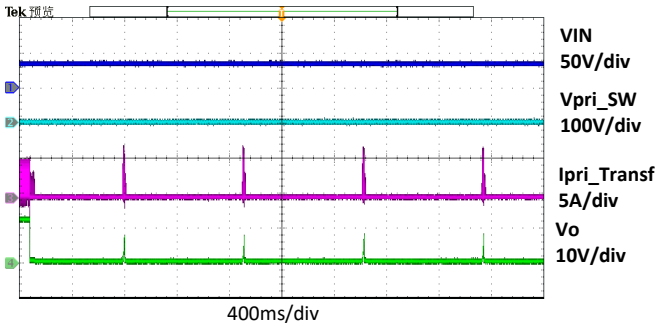
Steady State
(48V_{IN}, 12V_{OUT}, I_{OUT} = 6A)



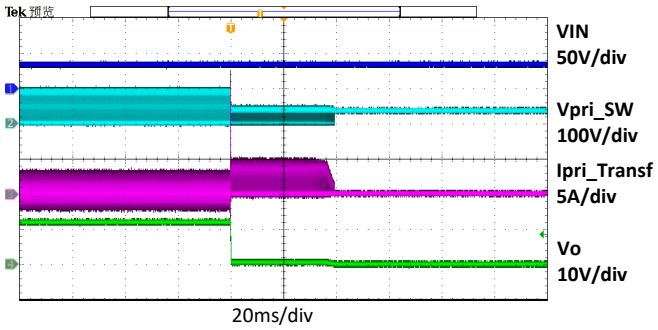
Dynamic Load Performance
(48V_{IN}, 12V_{OUT}, Load Step from 3A-6A-3A)



OCP Performance
(36V_{IN}, 12V_{OUT} from 6A to OCP)



Short Circuit Performance
(36V_{IN}, 12V_{OUT}, I_{OUT} from 0A to Short)



Functional Block Diagram

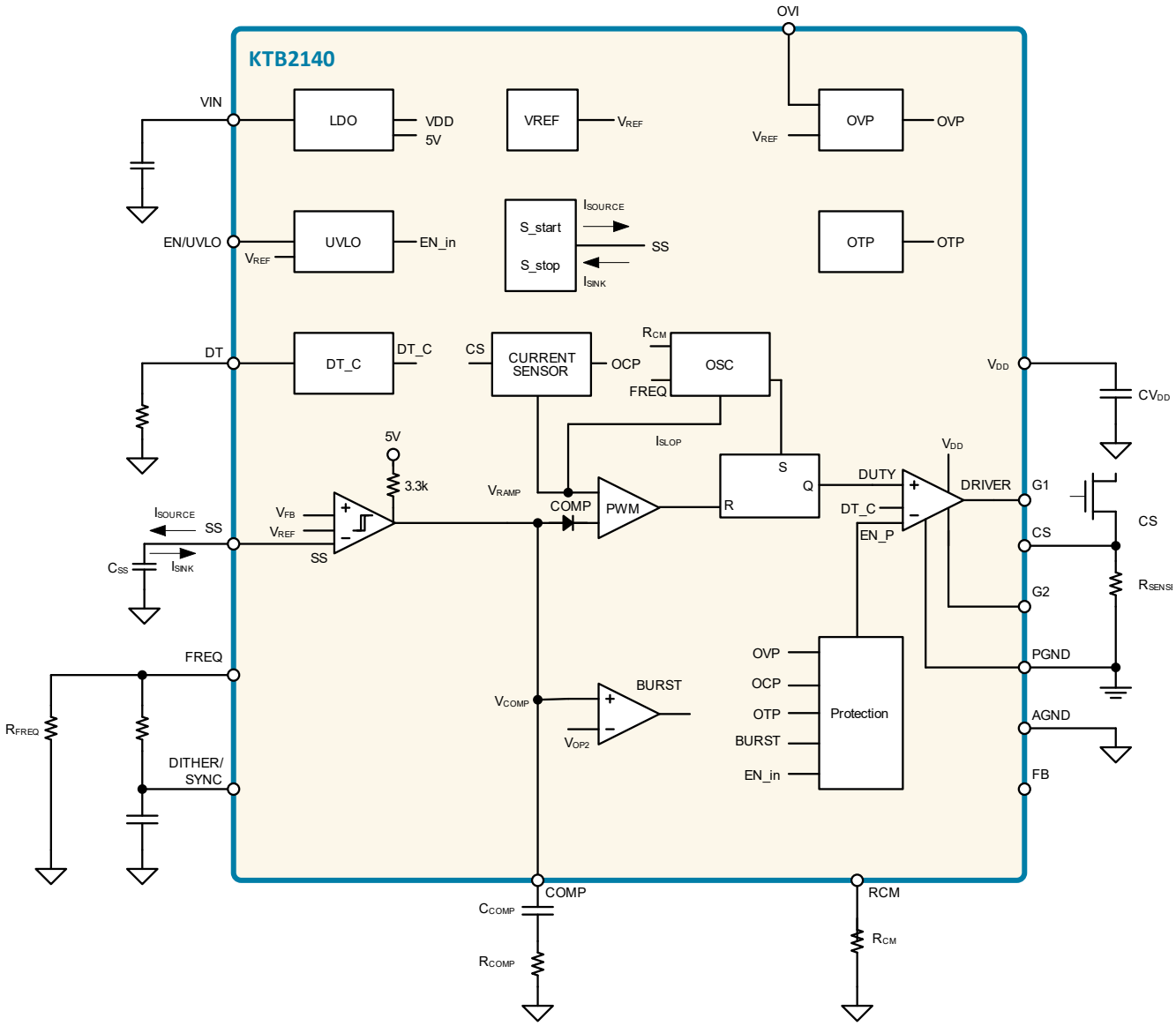


Figure 1. Functional Block Diagram

Functional Description

Overview

The KTB2140 is a peak current mode active clamp PWM controller that integrates all the circuitry required to design a smart and efficient converter for PoE and telecom mid-power DCDC converter applications.

KTB2140 features a programmable oscillator for the switching frequency, adjustable slope compensation, dual low-side drivers with programmable dead time, programmable soft-start, programmable frequency dithering, maximum duty limit, and a self-start internal high-voltage linear regulator.

Protection features include input EN/UVLO, input OVP, OCP, SCP, and OTP.

The KTB2140 is mainly used for active clamp forward/flyback converter applications for small and mid-power devices.

KTB2140 provides two control outputs, the main power switch control (G1) and the active clamp switch control (G2). The main output driver, G1, is designed for driving a forward/flyback converter primary MOSFET. The secondary output, G2, is designed for driving an active clamp circuit MOSFET, or a synchronous rectifier on the secondary side. In some low power applications, the KTB2140 can be configured for a simple RCD flyback converter where the secondary output, G2, is floating.

Enable (EN) / Under-Voltage Lockout (UVLO)

KTB2140 controller can be turned on and off using the EN/UVLO pin. If the EN pin is higher than its turn on threshold of 1.24V, the controller is enabled. Pulling the EN pin lower than its turn off threshold will disable the controller. The hysteresis voltage for EN pin is typically 80mV. Connecting a resistive divider between EN and VIN engages the input start-up voltage with hysteresis. The resistor from EN pin to ground is recommended to be smaller than 100K. Refer to Figure 2. To achieve a target input UVLO turn on point (V_{UVLO_On}), we can select R_{ENL} first (say 10K), then we can calculate the requested R_{ENH} by following the below Equation 1 to achieve this target input UVLO turn on point. After we get the values of R_{ENL} and $R_{ENH,}$ we can calculate the input UVLO turn off point by following Equation 2 below.

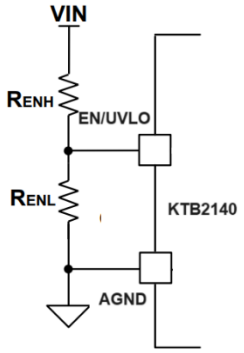


Figure 2. Configuring the Input UVLO Threshold through EN/UVLO Pin

$$R_{ENH} = \frac{(V_{UVLO_{On}} - 1.24) * R_{ENL}}{1.24}$$

Equation 1.

$$V_{UVLO\_Off} = (1.24 - 0.08) * \frac{R_{ENL} + R_{ENH}}{R_{ENL}}$$

Equation 2.

1.24 is the typical turn on threshold (1.24V) of EN/UVLO pin while 0.08 is the typical hysteresis voltage (80mV)

The EN pin maximum rating voltage (100V) allows it to connect to VIN pin for simple control. To prevent noise, it is recommended to connect a capacitor (> 1nF in most case) on the EN pin to AGND. If not used, connect this pin to a high logic or directly to VIN.

OVI

KTB2140 controller can achieve input over voltage detection and protection by using the OVI pin. A resistor divider from VIN to AGND can program the system OVP function. Fixed hysteresis of 100mV is included. If the OVI pin voltage reaches its typical OVP threshold of 1.13V, the controller will shut down. Connecting a resistive divider between OVI and VIN sets the input over voltage protection voltage with hysteresis. Please refer to Figure 3. To achieve a target input OVP turn off point (V_{OV_Off}), we can select R_{OVL} first (say 10K), then we can calculate the requested R_{OVH} by using Equation 3. to achieve this target input OVP turn off point. After we get the values of R_{OVL} and $R_{OVH,}$ we can calculate the input OVP restart turn-on (V_{OV_On}) point by following Equation 4.

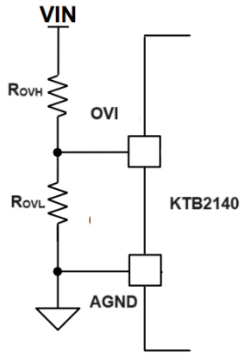


Figure 3. Configuring the Input OVP Threshold through OVI Pin

$$R_{OVH} = \frac{(V_{OV\_Off} - 1.24) * R_{OVL}}{1.24}$$

Equation 3.

$$V_{OV\_On}(V) = 1.13 * \frac{R_{OVL+}R_{OVH}}{R_{OVL}}$$

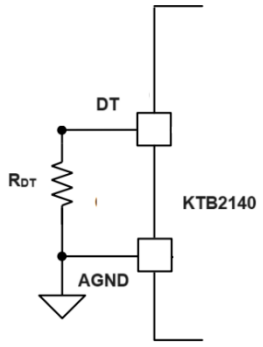
Equation 4.

1.24 is the typical OVP threshold of OVI pin rising while 1.13 is the OVP threshold of OVI pin falling.

To prevent noise, it is recommended to connect a capacitor (>1nF in most cases) on the OVI pin to AGND. If not used, please connect this pin to AGND.

DT

The relative phase of the main switch gate driver G1 and active clamp gate driver G2 can be configured for multiple applications for KTB2140. For default, the active clamp configurations utilizing a ground referenced P-Channel clamp switch, the two outputs should be in phase, with the active clamp output overlapping the main output. The dead time is controlled by the resistor value from DT pin connected to AGND pin of the controller. The rising edge dead time and the falling edge dead time are identical. The magnitude of the dead time can refer to the curve of Dead Time vs. Programming Resistance in the typical Characteristics part. The suggested DT resistance range is from 10K to around 220K. Please refer to Equation 5 for the roughly programmed dead time vs resistor.



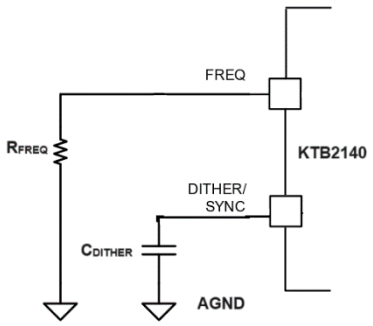
$$T_{DT}(\text{ns}) = 2.08 * R_{DT}(\text{K}\Omega)$$

Equation 5.

If DT pin is floating, the default dead time is around 60ns. The DT resistor should not be too far away from the chip.

FREQ

The oscillator frequency of KTB2140 is set by the external resistance connected between the FREQ and AGND pins. When the DITHER/SYNC pin is connected to AGND pin with a 10nF capacitor or connected to a 3.3V or 5V high logic voltage, the frequency dithering function will be disabled, the controller will run the frequency right at the settled oscillator frequency by FREQ pin.



Please refer to the Equation 6 below for the roughly programmed frequency and resistor:

$$R_{freq} = \frac{1}{F_{freq} * 4.2 * 10\hat{} - 11}$$

Equation 6.

For the programmed frequency details, please refer to the Switching Frequency vs. Programming Resistance curve in the typical Characteristics section.

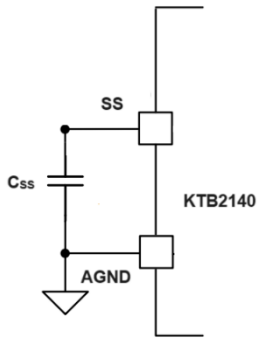
Soft Start /Soft Stop

The soft-start time is programmed by the capacitor (C_{SS})from SS pin to AGND. During startup, this capacitor is charged by a constant 10μA (I_{SS})current, and its voltage rises accordingly. This slowly rising voltage in the SS pin (V_{SS}) will limit the COMP voltage during startup. The COMP voltage is clamped around 0.8V higher than SS pin voltage during startup ($V_{COMP} = V_{SS} + 0.8$). This slowly rising and clamped voltage on the COMP will achieve soft start for DC-DC converter applications during startup. Soft start begins when V_{SS} is around 0.1V.

The soft start finishes when the clamped COMP voltage reaches a stable working voltage that is settled by the DC-DC converter.

Please refer to Equation 7 for the programmed capacitor (C_{SS}) and the soft startup time (T_{START}).

V_{SS} is the SS pin voltage that the soft start finished. For a typical application with 100nF C_{SS}, the soft startup time is around 10mS.



$$C_{SS} = \frac{I_{SS} * T_{START}}{V_{SS}}$$

Equation 7.

To prevent oscillations in the self-driven synchronous rectifiers on the secondary side of the converter during turnoff, the KTB2140 has a soft stop feature. When a fault OCP, UVLO, OVP, OTP, or turn off event occurs, the SS voltage falls slowly from 5V by a constant 10µA discharge current. When SS voltage drops to a certain voltage, it will start to clamp the COMP voltage (V_{COMP} =V_{SS} +0.8V). The COMP pin voltage is clamped around 0.8V higher than SS pin voltage during turn off which lets the COMP voltage slowly drop and the DC-DC converter can achieve soft stop. The soft stop finishes when SS pin voltage (V_{SS}) drops to approximately 0.2V. Then the controller will fully turn off. The soft stop time is similar as the soft startup time if ignoring this 0.2V.

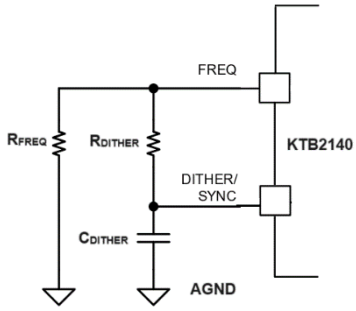
DITHER / SYNC

The KTB2140 has a Frequency Dithering Programming and Synchronization function. When DITHER/SYNC pin is configured to the Frequency Dithering Programming function, the switching frequency of the converter can be dithered by connecting a capacitor from DITHER/SYNC pin to AGND, and a resistor from DITHER/SYNC pin to FREQ pin. This results in lower EMI.

A current source at DITHER/SYNC charges the capacitor C_{DITHER} to 2V with 50µA (I_{DITHER}). Upon reaching this trip point, it discharges C_{DITHER} to 0.4V with 50µA. The charging and discharging of the capacitor generates a triangular waveform on DITHER/SYNC with bottom and peak levels at 0.4V and 2V. The triangular waveform frequency (modulation frequency) can be programmed by the capacitor from DITHER/SYNC pin to GND.

The resistor (R_{DITHER}) connected from DITHER/SYNC to FREQ determines the amount of dither frequency from FREQ pin settling the oscillator frequency. The approximate dither frequency range can be calculated using Equation 8 below. Please refer to Equation 9 for the triangular waveform frequency (modulation frequency).

If setting R_{DITHER} to 5 times R_{FREQ}, it will generate around +/-13.3% dither frequency of settled oscillator frequency. If setting C_{DITHER} to 10nF, it will generate 1.56K modulation frequency.



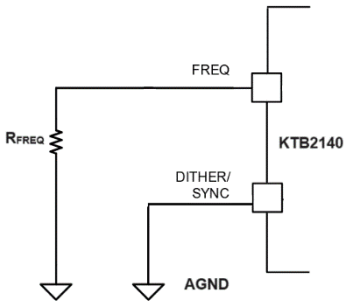
$$Freq_{DITHER\ Range}(+/-\%) = \frac{2}{3} * \frac{R_{FREQ}}{R_{DITHER}} * 100\%$$

Equation 8.

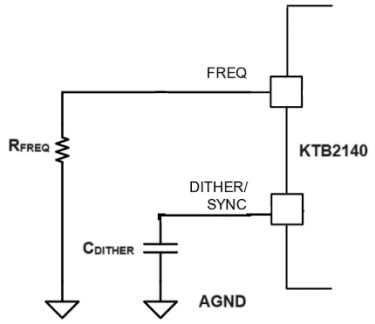
$$Freq_{Modulation} = \frac{1}{2} * \frac{I_{DITHER}}{C_{DITHER} * 1.6}$$

Equation 9.

When DITHER/SYNC is connected to AGND pin directly, there will exist a default Frequency Dithering function. The frequency dithering is fixed at ±7% of FREQ pin settled oscillator frequency. The default modulation frequency is 1/64 of FREQ pin settled oscillator frequency.



When DITHER/SYNC is connected to AGND pin with a 10nF capacitor or connected to a 3.3V or 5V high logic voltage, the frequency dithering function will be disabled.



When DITHER/SYNC pin is configured to the Synchronization function this pin provides an input for an external-clock signal which synchronizes the internal oscillator of the KTB2140 controller. This pin should connect to external clock signal directly without any other components.

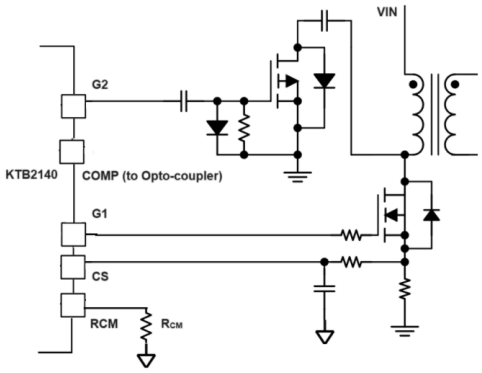
The external synchronizing frequency is suggested to be in the 110% to 130% range of the free-running frequency set by the FREQ pin resistor. The acceptable minimum pulse-width of the synchronization signal is approximately 400ns (positive logic). The synchronization signal high level should exceed 2.9V.

PWM Comparator and Slope Compensation

In a typical isolated flyback/forward topology application, the error amplifier is located outside the IC and the feedback signal is taken on the collector of an optocoupler, while the current is sensed through a current sense resistor Rcs connected between the source of the primary Main Switching MOSFET and the PGND.

The sensed voltage on the CS pin is then amplified and fed to the PWM comparator for current mode control. The current comparator takes this amplified current sensed voltage (plus slope compensation) as one of its inputs, then compares this value with the voltage of VCOMP-0.8V.

The COMP is internally pulled up to a fixed reference of 5V using an internal 3.3KΩ resistor. The PWM comparator start to output gate driver signals when the voltage at the COMP pin rise to approximately 1.0V. The comparator stop to output gate driver signals when the COMP pin voltage drops below 1.0V. For duty cycles greater than 50%, current mode control loops are subject to sub-harmonic oscillation. The controller fixes the maximum duty cycle at around 80% and implements a slope compensation technique consisting in adding a fixed slope voltage ramp to the signal sensed at the CS pin. This slope compensation is achieved by adding an external resistor from RCM pin to AGND (Refer below figure).

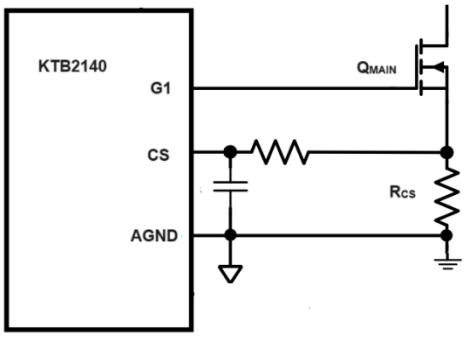


CS

The CS pin input provides a control ramp for the pulse width modulator and current limit detection for overload protection.

The KTB2140 is a peak current mode active clamp controller. The current through the external Main MOSFET can be sensed through a current-sense resistor that is connected in series with the MOSFET's source. The sensed voltage on the CS pin is then amplified and fed to the PWM comparator for current mode control. The current comparator takes this amplified current sensed voltage (plus slope compensation) as one of its inputs, then compares this value with the VCOMP-0.8V. When the voltage exceeds VCOMP-0.8V, the comparator outputs low, and the power MOSFET turns off.

If the sensed voltage at CS exceeds 0.3V and stays around 32 cycles, the over-current protection will trigger and enter soft stop. A small RC filter, located near the controller, is recommended for the CS input pin. The blanking time is around 65ns at the start of each main switch cycle to attenuate the leading-edge spike in the current sense signal. After soft stop, the KTB2140 will restart after the hiccup time. The hiccup time is around (34,000) times of the oscillator switching cycle settled by the FREQ pin resistor.



G1 / G2

The KTB2140 has two integrated MOSFET drivers with up to 1.5 A peak source and sink current capability. G1 is intended for driving the main switching MOSFET, while G2 is used for an auxiliary function, depending on the topology selected. For typical application, G2 will control a P-channel auxiliary MOSFET referred to PGND in active clamp forward topologies. The dead time is controlled by the resistor value from DT pin connected to AGND pin of the controller. The rising edge dead time and the falling edge dead time are identical (refer to Figure 4). DT can be adjusted to fine tune the relative switching times of the MOSFETs and to maximize the converter efficiency.

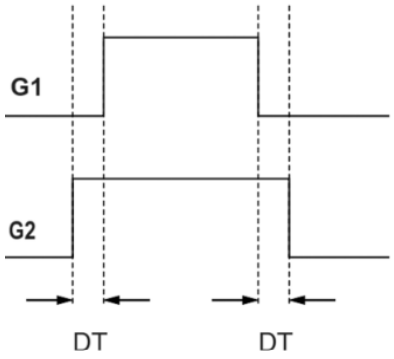


Figure 4. Time Relation between Output Drivers and DT

VDD

There is an internal high voltage start-up regulator in the KTB2140. It allows the Vin pin to be connected directly to a wide range DC line voltage up to maximum 100V. The VDD voltage is regulated to around 10V when Vin is over 14V and VDD voltage is around Vin-1.3V when Vin in the range of 6V to 14V. The VDD regulator provides power to internal gate drivers. The typical recommended capacitance for the VDD regulator is 1 µF.

When in the high input voltage applications (say over 36V), to save power loss in the internal start-up regulator and prevent the whole KTB2140 controller to be too hot, an external regulated voltage supply is suggested to apply to the VDD pin. This external voltage regulator is usually from the auxiliary transformer winding. The external regulated voltage at the VDD pin is suggested to be greater than 11 V that can shut off the internal start-up regulator and not exceed 15 V to over the maximum rating of the VDD pin.

Thermal Limit / Protection

The KTB2140 provides thermal protection by the continuous monitoring of the die junction temperature. The thermal protection limit is set to around 150 °C on the junction temperature and is always active. When this threshold is exceeded, the controller is switched-off following the soft-stop method. When the junction temperature goes below about 130 °C, the controller will restart automatically doing a startup phase and without needing to recycle the input voltage.

Applications Information

Application Circuits

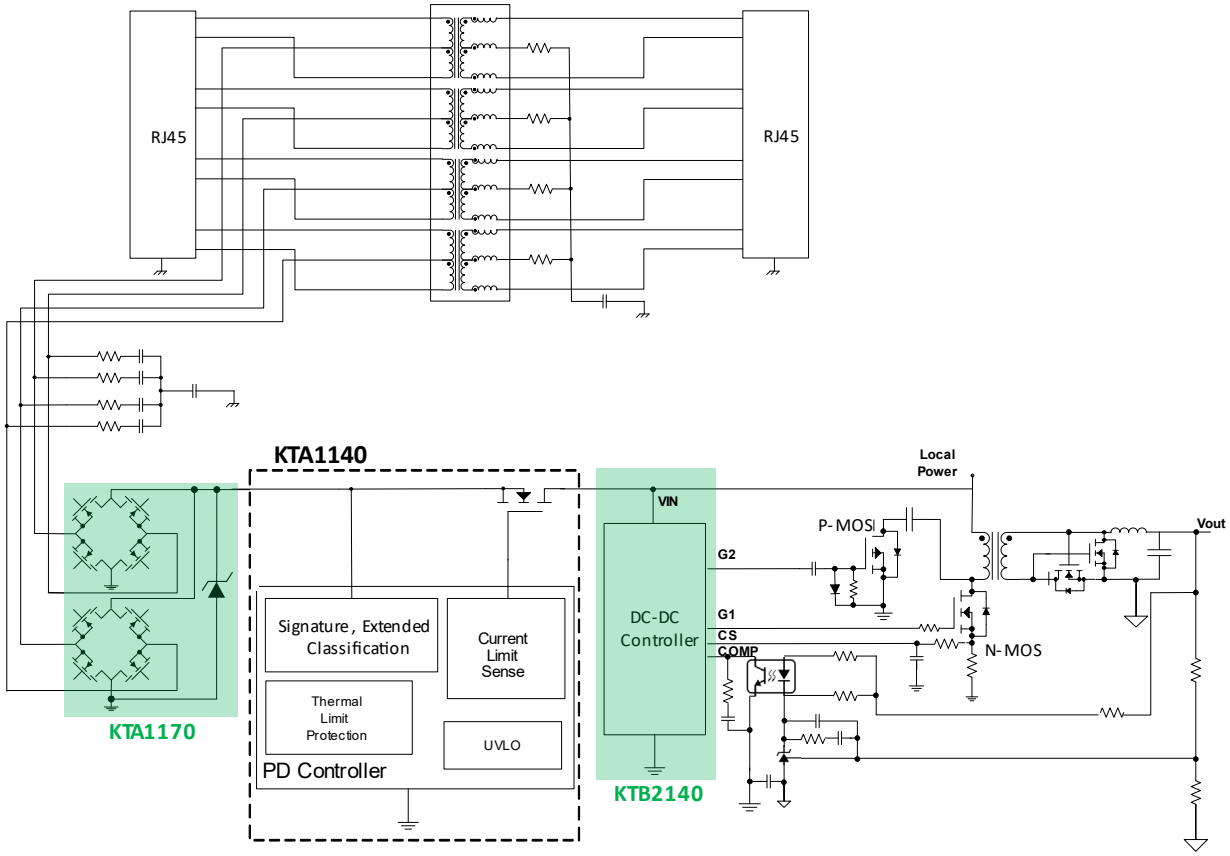


Figure 5. High-Efficiency Active Clamp Forward Solution for Higher Power Applications[11]

[11] This is a simplified conceptual schematic. Please refer to the reference design documentation for detailed design and component information.

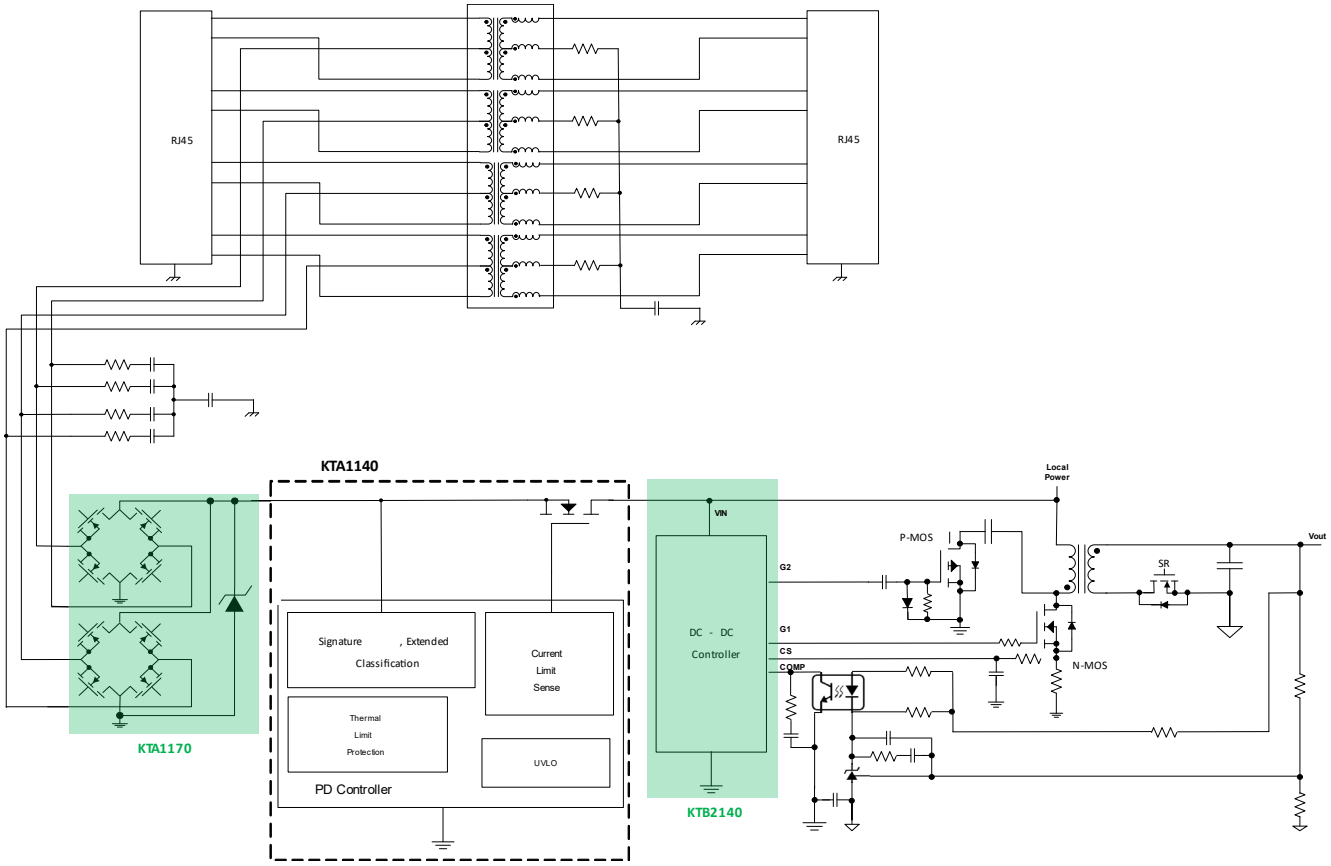


Figure 6.High-Efficiency Active Clamp Flyback Solution for Middle Power Applications[12]

[12] This is a simplified conceptual schematic. Please refer to the reference design documentation for detailed design and component information.

Application Topologies

KTB2140 can be used in many high efficiency DC-DC topologies such as the following:

- Flyback, Forward
- Flyback with synchronous rectification
- Flyback with active clamp
- Forward with active clamp

Typical application circuits of the KTB2140 are shown above.

For a typical 48V input bus to 12V output active clamp forward converter design by KTB2140, the target output power range is from around 50W to around 200W.

For a typical 48V input bus to 12V output active clamp flyback converter design by KTB2140, the target output power range is from around 30W to around 50W.

For a typical 48V input bus to 12V output RCD flyback converter design by KTB2140, the target output power range is suggested to be smaller than 30W.

For all these applications, besides control components design, we need to also select suitable power components such as MOSFET, transformers, output rectification diode, inductors and so on. Among these components, the transformer design is the most complex. Below, introduces the key design procedures of the transformer for the application circuits of KTB2140.

Forward Transformer Design

The forward transformer design should consider the input voltage, output voltage, output current and transformer size and so on. The key parameters of the transformer are turns ratio, winding turns, current rating, and core selection. For the forward transform design, we usually design the turns ratio first, then we design the primary winding turns of the transform, and finally design the secondary winding turns of the transform. Below is reference design of the key procedure for a forward transformer design.

Step 1:

For the forward transformer design, we design the turn ratio of transform first according to the equation as follows:

$$N = \frac{Vin\_\min * Dmax}{Vo_{max}}$$

Where,

N = the turns ratio from primary winding (Np) to secondary winding (Ns)
Vin_min = the min. operating input voltage
Vo_max = the max. output voltage
Dmax = max. duty cycle, (D_{max} is approximately 45% for most narrow input range application, Dmax is approximately 70% for a wide input range application. A narrow input range application is usually smaller than 2 times (from $36V_{IN}$ to $60V_{IN}$). A Wide input range application is usually over 4 times (from $18V_{IN}$ to $75V_{IN}$).

We can choose the suitable D_{max} and the desired V_{IN} and V_{OUT} to finish the turn ratio design first.

Step 2:

This step we will design the primary winding turns of transforms according to the equation as follows:

$$Np = \frac{Vin * D}{Fsw * \Delta B * Ae}$$

Where,

Np = the turns of primary winding
Vin = the operating input voltage
Fsw = Switching frequency
ΔB= maximum AC flux density (ΔB <0.3 in most cases)
Ae= cross-sectional area of the core
D = Duty cycle

For the KTB2140 typical DC-DC forward converter applications, FSW, around 350KHz, will get a good balance between converter size and system performance. Select the right Ae according to the output power of transform. Then we can finish the primary winding turns (Np) design.

In the forward DC-DC converter application, when the power MOSFET turns on, the forward transformer transfers energy to the output, while V_{IN} generates a primary-side inductance current in the transformer.

There must be enough primary winding turns to prevent the transformer from saturating.

Step 3:
After designing n, Np, then we can design the turns of secondary winding and evaluate the core loss, winding loss of the transform.

The parameters of the transformer design should consider turns ratio, winding turns, switching frequency, power MOSFET and diode voltage stress and so on. We need to tune the n, Np, Fsw and so on to get a good balance of the transform parameters for the total system design.

Flyback Transformer Design

The flyback transformer design should consider the input voltage, output voltage, output current and transformer size. The key electrical parameters of the transformer are turns ratio, inductance, saturation current and so on. For the flyback transform design, we usually design the turns ratio first, then we design the inductance of the transform, and finally design the saturation current of transform. Below is reference design of the key procedure for a flyback transformer design.

Step 1:
The transformer turns ratio is calculated as follows:

$$N = \frac{Vin\_min * Dmax}{(Vomax + Vd) * (1 - Dmax)}$$

Where,

N = the turns ratio from primary winding to secondary winding
Vin_min = the min. operating input voltage
Vo_max = the max. output voltage
Vd = the forward voltage drop of secondary rectifier diode.
Dmax = max. duty cycle, (Dmax is approximately 45% for most narrow input range application, Dmax is approximately 70% for wide input range application)

We can choose the suitable Dmax and the desired Vin and Vo to finish the turn ratio design first.

In most narrow input DC-DC applications (from 36Vin to 72Vin), n is around 2 for a 12Vo application while n is around 5 for a 5Vo application.

Step 2:

After designing n, then the flyback transformer primary inductance is calculated as follows:

$$Lm = \frac{N * Vin_{min} * D * (1 - D)}{Fsw * Io * Kc}$$

Where,

Lm = the primary inductance of flyback transformer
N = the turns ratio from primary winding to secondary winding
Vin = the operating input voltage
D = duty cycle.
Fsw = Switching frequency
Io = Output current
Kc = is the ripple current coefficient compared with output current. The value of Kc is normally selected between 0.5 to 1.5.

For the KTB2140 typical DC-DC flyback converter applications, choosing an FSW around 350KHz will get a good balance between converter size and system performance. Choose the suitable Fsw, Kc, and the desired Vin and Io can finish the Lm design.

Step 3:
Calculated primary side peak current is calculated as follows:

$$Ipeak = \frac{Io}{N * (1 - D)} + \frac{Vin * D}{2Fsw * Lm}$$

Where,

Io = Output current
n = the turn ratio from primary winding to secondary winding
D = duty cycle
Vin = the operating input voltage
D = duty cycle
Fsw = Switching frequency
Lm = the primary inductance of flyback transformer

After designing Lm, then we select the right Ae according to the output power of transform. Next, we can finish the winding design. There must be enough primary winding turns to prevent the transformer from saturation.

The transform parameters need to be comprehensively considered by choosing the correct turns ratio, winding turns, switching frequency, power MOSFET and diode voltage stress and so on. These parameters need to be tuned to get a good balance of the transformer for the total system design.

PCB Layout Guidelines

Thermal De-Rating and Board Layout Considerations

The KTB2140 is capable of operating to an industrial temperature range of 85°C in ambient air and up to 125°C junction temperature, without forced cooling. A thermal pad on the underside of the package dissipates the heat generated by the PD die.

In higher power applications, designers must consider thermal dissipation as an integral part of their system architecture and plan to remove heat via this pad.

If the PCB landing pattern is properly designed, the WQFN package should exhibit a thermal resistance of

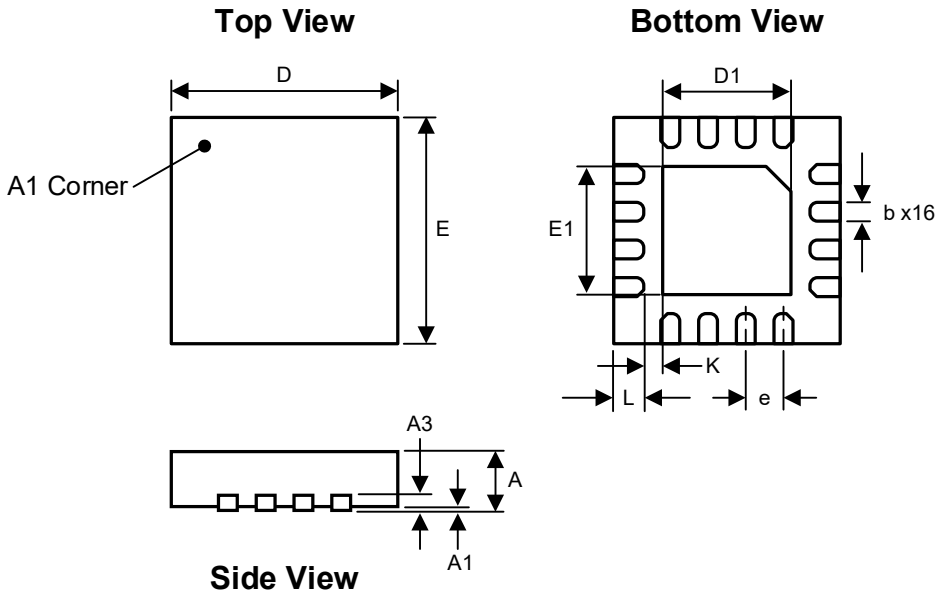
ΘJA ≈ 76°C/W. For adequate heat dissipation, the board layout must include a ground pad which provides both the ground connection and dissipates the heat energy produced in the chip. Thermal vias are used to draw heat away from the PD package and to transfer it to the backside of the system PCB.

Besides the layout for thermal consideration, the following layout guidelines are recommended for optimum system performance.

1. Keep below power stage loops area as small as possible for minimal noise and ringing.
    a. Input power loop: Input capacitors, Primary of Transformer, Main MOSFET, Current sense resistor.
    b. Output power loop: Secondary of Transformer, Output capacitors, Rectifier Diodes or MOSFETs.
    c. Active-clamp loop: Input capacitors, Primary of Transformer, active-clamp MOSFET and Capacitor.
2. The KTB2140 has an analog/signal ground, AGND (Pin11), and a power ground, PGND (Pin12). AGND is used for analog/signal connections such as FREQ, DT and other signal pins. PGND is used for high power connections such as the output drivers, G1, G2 and VDD pins. All the analog/signal ground tracks should be connected in common near the IC AGND (Pin11), and then a single connection made from the KTB2140 signal ground to the system power ground (sense resistor ground point).
3. The current-sense circuit usually employs a sense resistor. The sense resistor is connected between the Source of Main MOSFET and the power ground terminal of the system. A low inductance resistor should be used. The negative terminal of the input power capacitor, the ground return of the MOSFET, and current-sensing resistor should be close together. The filter network for the current-sense circuit should be located close to the IC.
4. The gate drive outputs of the KTB2140 should have short direct paths to the MOSFETs to minimize inductance in the PCB traces, wider trace is suggested for these gate drive loops.
5. Place all the components (VDD pin capacitor, DT pin resistor, etc.) to their respective grounds and place these components close to the IC to decouple noise. These components and traces should keep far away from the noise nodes (such as primary Main MOSFET switching node).

Packaging Information

WQFN33-16 (3.00mm x 3.00mm x 0.75mm)



Dimension	mm		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF		
b	0.18	0.25	0.30
D	2.90	3.00	3.10
D1	1.65	1.70	1.75
E	2.90	3.00	3.10
E1	1.65	1.70	1.75
e	0.50 BSC		
K	0.20	–	–
L	0.35	0.40	0.45

Recommended Footprint